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WORKING DOCUMENT

From:	General Secretariat of the Council
To:	Working Party on Competitiveness and Growth (Industry)
Subject:	Proposal on Chips Act 2.0 – Presentation by the Commission on Pillar I and II of the proposal



Chips Act 2.0

Pillar I & II

Working Party on Competitiveness and Growth (Industry)
8 July 2026

Microelectronics and Photonics
DG CNECT C.3
European Commission



Pillar I

Articles 7 – 12

Potential Grand Challenges under the Initiative 2.0

1. Energy-efficient computing infrastructures

- New computing technologies for drastic ($\times 1000$) energy reduction
- Energy-efficient, secure and distributed AI infrastructures
- High-performance AI accelerators (HBM-class memory, stacked logic, optical/RF interconnects)
- Contextual edge intelligence and secure low-power infrastructures

→ **Linked to CADA Grand Challenge 1:** energy- and resource-efficient compute infrastructure

2. European cloud & AI stack autonomy

- EU-designed (and where appropriate EU-manufactured) processors and accelerators
- Integration into a European cloud and AI stack
- Support for solutions developed by startups and innovation procurement

→ **Linked to CADA Grand Challenge 2:** autonomy across the cloud and AI stack / eliminating dependencies in critical technologies



Potential Grand Challenges under the Initiative 2.0

3. Physical AI and autonomous systems

- Foundational technologies for autonomous systems (e.g., humanoid and industrial robots)
- Applications from med-tech and healthcare to manufacturing, aerospace and defence
- R&I in physical AI should advance mainstream technologies, e.g., in power semiconductors, microcontrollers, analogue/mixed-signal and sensor technologies

→ **Linked to CADA Grand Challenge 4:** advanced physical AI models and systems

4. Smart glasses and virtual worlds

- Optics, photonics and semiconductor technologies are crucial for sensing and visualization devices
- Grand Challenge should integrate ultra-low power components into smart-glasses prototypes and demonstrators
- Components include sensors, displays, lasers, specialty glasses and neuromorphic/AI chips
- Objective of achieving significant improvements in processing and communication of Virtual Worlds content



Potential Grand Challenges under the Initiative 2.0

5. Other types of Grand Challenges

- Addressing market targets, e.g., taping out chips from 100 fabless startups including 10 unicorns by 2035
- Addressing lead markets and demand stimulation, e.g., by developing automotive hardware platforms or the full stack for AI (Giga) Factories
- Address new semiconductor production technologies, e.g., increasing recycling and boosting circularity of materials, or the development of advanced semiconductors cooling technologies



Example of Demand Accelerator (Article 8)

Joint work between the Semiconductor Alliance and the European Connected and Autonomous Vehicle Alliance (ECAVA)

- Stemming from the **Action plan on the future of the automotive sector** (COM(2025)95)
- The development and scaling of a competitive and sovereign European automotive semiconductor ecosystem demands **extreme investments, and no single player or Member State in Europe is likely to succeed alone.**
- Rather than focusing on isolated hardware development, Europe must drive the **fast vertical integration of technology together with the Automotive OEMs.**
- Tight, early-stage collaboration between European semiconductor innovators, automotive suppliers and automotive OEMs is critical to accelerate the cycle from processor and chiplet design to deployment.
- Common working group between the Semiconductor Alliance and ECAVA developing an Automotive Hardware Platform Roadmap for Software Defined Vehicles.



Example of Demand Forum (Article 9)

The supply-demand matchmaking platform

- The overall goal of the Demand Forum - to ensure that **European chips manufacturing is better aligned with and can answer industrial demand.**
- The **Demand Forum** will allow European semiconductor technology initiatives (ESTi) and Strategic projects to **showcase** their technological capabilities and proposed solutions.
- Will be implemented by the Industrial Alliance for Semiconductors.
- A possible implementation example could be the **EU Energy and Raw Materials Platform**, which offers solutions to **collect demand, and supply offers from companies** and provide aggregation and **matchmaking** services, potentially leading to joint purchasing for a wide range of energy-related products and strategic raw materials.



Chip Innovation Procurement (Article 10)

- Demand-side measure (not a new procurement rule)
- **Aim:** to create a structured European demand for innovative semiconductors and support their first integration and deployment in real-world applications
- The objective is to bridge the gap between semiconductor innovation and market uptake, ensuring that innovative chips developed in Europe are effectively integrated into downstream applications and deployed at scale
- The Chips JU could act as an enabler and facilitator (legal guidance, procurement support, etc.), rather than as the actual purchaser, supporting public and private buyers in procuring, integrating, and deploying innovative semiconductor-based solutions
- The instrument would help aggregate demand across borders, including through joint procurement arrangements and the creation of buyer groups, thereby providing stronger market signals to European chip suppliers.
- Beyond procurement, the instrument would support the integration and first deployment of innovative chips, including redesign, software porting, testing, certification, validation, and ramp-up activities



Pillar II

Articles 13, 20, 14, 15, 19
– time allowing; Articles 16 – 18

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Article 13 – Public interest and public support

*Relevant **recitals**: (38), (39), (40).*

Very similar Article [Article 16] in Chips Act “1”, now with additions made related to strategic projects and support via, among others, the European Competitiveness Fund.

- Public interest recognition for European semiconductor technology initiatives and strategic projects; read in conjunction with Article 21(4) ‘status of highest national significance’.
- Support by:
 - Member States, to **European semiconductor technology initiatives** and **strategic projects**, which may provide financial support measures and administrative support; support must comply with Articles 107-108 TFEU (State aid rules).
 - European Commission to **strategic projects**, which may provide financial support measures and administrative support; support must comply with Articles 107-108 TFEU (State aid rules).



Article 20 – Coordination of financing

- The Commission and the European Semiconductor Board (= Member States) support European semiconductor technology initiatives and strategic projects secure funding by **coordinating investors, identifying financing sources, and providing tailored funding guidance.**
- The **European Commission** may:
 - coordinate activities to attract and mobilize investments ("crowd-in" funding) for European semiconductor technology initiatives and strategic projects;
 - support projects that face difficulties accessing financing.
- Activities are carried out in synergy with EU funding programmes and remain subject to State aid rules (Articles 107–108 TFEU);
- The **European Semiconductor Board** may:
 - provide financing advice upon request from a European semiconductor technology initiative or strategic project



Articles 14 and 15 – European semiconductor technology initiatives ('ESTIs') / application for status

*Relevant **recitals**: (43) to (49) for Article 14, (50 and (51) for Article 15.*

Very similar Articles [Article 13 - 14] in Chips Act “1” for ‘integrated production facilities’ (IPF) and ‘open EU foundries’ (OEF). In Chips Act 2.0:

- **Simplification** by merging IPF/OEF into one concept of ‘**European semiconductor technology initiatives**’ (‘ESTIs’)
- Additional paragraphs;
 - ESTIs shall be domestic undertakings;
 - ESTIs shall demonstrate they will reduce supply chain dependence on non-domestic undertakings and strengthen the Union’s security of supply (Article 14(2); and contribute to indispensability, resilience, prosperity and security of supply (Article 14(3)).
 - To clarify in Chips Act 2.0: First-of-a-kind initiatives do not have to receive support measures (State aid) or administrative support to apply for ESTI status (Article 14(5)).
- Requirements for ESTIs remain the same as in Chips Act “1”; apart from participation in the Business-to-Business Supply Chain Platform [Article 34].
- Article 15 (Application for status as European semiconductor technology initiative) remains unchanged from the procedure for integrated production facilities (IPF) and open EU foundries (OEF) in Chips Act “1”.



Article 19 – Advanced semiconductor manufacturing

Relevant recital: (56)

- The article is presented to highlight a relevant example of a *Strategic Project* the Commission considers of **high priority** for strengthening Union **sovereignty** and **security of supply** in semiconductors, not as a predetermined outcome.
- This reference reflects the potential **strategic importance** and possible **scale** of resources required for such an Open Foundry project, ensuring **transparency** towards Member States from the outset. It does not preempt in any way collaborative discussions on framing, implementation, participating actors, or funding arrangements, which remain fully open.
- Notably, the project is conceived as a coordinated **multi-site** network **distributed across the EU**, ensuring that investments benefit the broader supply chain (connecting different hubs for manufacturing, advanced packaging, substrates, equipment, design etc.). Securing these end-to-end capabilities is essential to eliminate persistent **critical dependencies** and intercept relevant **technology trends** (e.g. chiplet integration).
- The project is designed to take into account the requirements and objectives of potential offtakers (Article 8), ensuring **alignment** with the real needs of **European industry**.



Article 16 – Strategic projects

Relevant recitals: (52) to (55).

- Article 16(1) sets out the **criteria** for recognition as a strategic project by the Commission;
 - (a) it provides significant added value to the Union by substantially contributing to **objectives of common Union interest**;
 - (b) the strategic project is carried out by **domestic undertakings**;
 - (c) strategic projects shall demonstrate that they will articulate their supply chain in a way that reduces supply chain dependence on non-domestic undertakings and strengthen the Union's security of supply – [similar as for ESTIs in Article 14(2)];
 - (d) it has a clear cross-border dimension, in particular through **technical cooperation or public support** involving **more than one Member State**; -- [the cross-border dimension is not just about public funding];
 - (e) it contributes to the **resilience** and robustness of the Union's **semiconductor value chain**;
 - (f) it contributes to strengthening the Union's technological sovereignty and technological leadership by enabling, advancing or securing critical capacities, technologies or capabilities within the Union, including by reducing **strategic dependencies**.
- Strategic projects may be multi-site, but are still to be operated by a single consortium that functions as an integrated legal and technical entity (Article 16(2)).
- Participation is limited to Union entities (Article 16(3), although Article 16(4) allows for derogation from this rule.



Article 17 – Identification of priority areas for strategic projects

Relevant **recital**: (56), relevant **Annex**: Annex II

Annex II provides a technical description of **priority areas for potential strategic projects**.

The Commission may update Annex II through delegated acts. Updates may be made to reflect technological developments and market changes in the semiconductor sector.

Taking into account the opinion of the **European Semiconductor Board** (= Member States) and the criteria for strategic projects [Article 16(1)], the Commission may **identify and update the indicative technology areas** for strategic semiconductor projects in Annex II, ensuring that EU priorities remain aligned with technological progress and market developments.



Article 18 – Designation of strategic projects

*Relevant **recitals**: (57) to (59)*

- Implementation of actions supporting strategic projects is **entrusted to the Chips Joint Undertaking** and carried out through actions set out in its work programme (Article 18(1));
- It is the **Commission** – taking into account the opinion of the European Semiconductor Board – that **designates** proposals selected for funding by the Chips Joint Undertaking as **strategic project** via decision. Strategic projects should comply with the criteria of Article 16(1) and have to request designation as such.
- Projects not selected for funding may also be designated as strategic project if this is indicated in the call for proposal / related application procedures and should be requested by the project (Article 18(3)).
- Strategic projects **may also be first-of-a-kind initiatives**. If a strategic project also qualifies as first-of-a-kind, the Commission decision under paragraph 2 shall indicate this as such (Article 18(4)).
- Strategic projects benefit from the **same rights and are subject to the same obligations** as ESTIs under Article 14(6).
- The designation as strategic project may be **reviewed / withdrawn** (Article 18(7)(8)(9)).



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Thank you!