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COVER NOTE

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PART 3/4

COMMISSION STAFF WORKING DOCUMENT

A Chips Act for Europe

6. Evolution of Technology to Meet the needs in 2030

6.1 Greater Processing Power

The demand for leading edge chips is forecast to grow much faster than trailing edge chips (See Figure 18). In terms of number of transistors per device this is expected to rise from 100 billion transistors today to 1 trillion transistors by 2030.

The explosion in demand for semiconductors is being driven by ubiquitous computing, the shift towards edge computing, pervasive connectivity and AI applications, which are transforming the world. This in turn requires lower latency, higher density, and more power-efficient processor solutions. To achieve this, **significant R&D investments will be required in new transistor designs, EUV tools, advanced packaging and precision manufacturing for the Angstrom Era of semiconductors**. This will have impacts on automotive, healthcare, retail, banking, etc., where digitalisation is driving radical change and disruption. Graphics and gaming, networking and data processing will all need increased performance, better efficiency, and lower power. The world creates nearly 270,000 petabytes (27×10^{19}) of data every day[1]. **Intel estimates that by 2030 on average, all of us will have 1 petaflop (10^{15} floating-point operations per second) of compute and 1 petabyte of data less than 1 millisecond away**[2]. This demand for more and more computing power will push the industry to maintain the pace of Moore's Law.

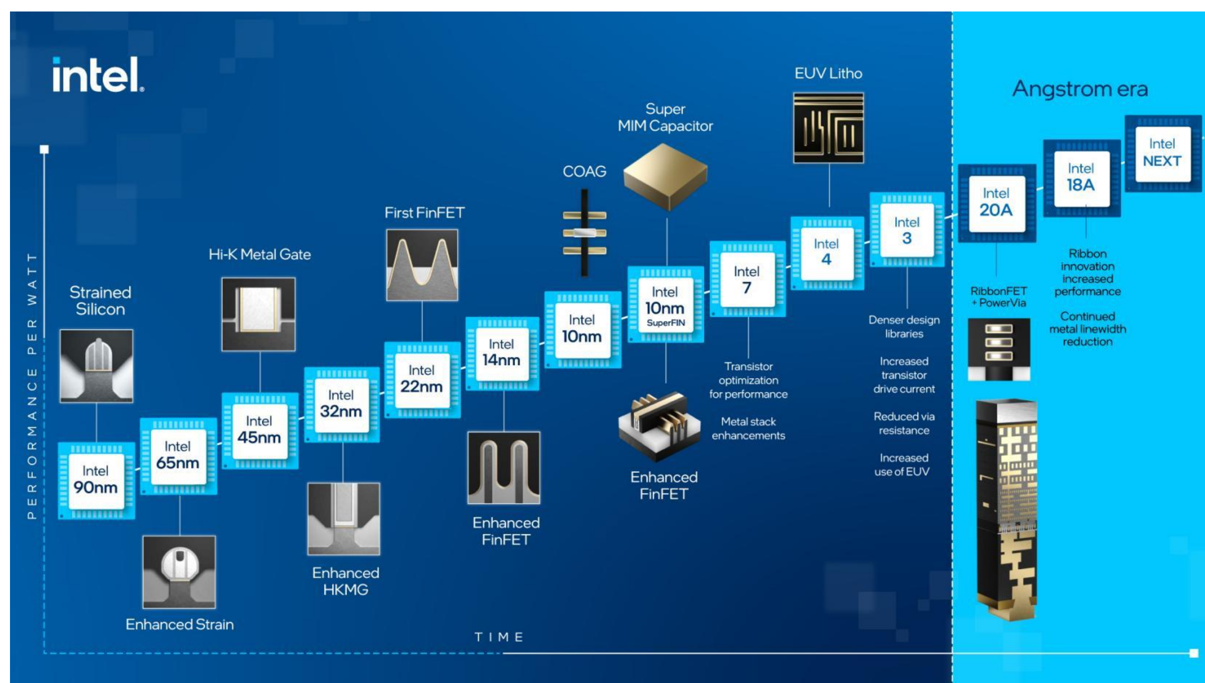

Figure 35. Process Changes and Reductions in Device Feature Size (Source: Intel)

To enable this progress, the industry needs to constantly innovate. As physical dimensions continue to shrink, advances are needed in materials science, new process architectures and design technology co-

[1] According to IDC, 267,906 Petabytes of data are generated every day

[2] Moore's Law - Now and in the Future © Intel corporation

optimization. For manufacturing, EUV lithography from ASML is being used to improve resolution and reduce errors. However, innovation is continuous and new processor nodes are under development to deliver additional gains in power, performance and density.

Successive generations of smartphones, servers and PCs will require ever-increasing computational throughput that can only be achieved at smaller node dimensions. When moving from one semiconductor manufacturing generation to the next there is a 10-15% gain in speed, 20-30% gain in energy efficiency and a reduction of silicon area of about 50% (see figure 36).

Technology generation	Speed gain at equal power	Energy efficiency gain at same speed	Gain in packing density (transistors/mm²)
5nm vs 7nm	15%	30%	x1.8
3nm vs 5nm	10-15%	25-30%	x1.7

Figure 36. Evolution of technology generations for semiconductor manufacturing (Source: TSMC)

Many industrial sectors, such as automotive, industrial automation, healthcare and communications, will make increasing use of AI and edge computing. Such applications will also increasingly drive demand at leading-edge nodes. AI chips require speed and efficiency to cope with vast amounts of data; if deployed at the edge (ie, directly on a device rather than in a remote data centre), better energy efficiency enables them to be integrated into handheld appliances or robots and perform AI tasks locally.

Another key aspect is 3D assembly and packaging. Up until the 2010s, these were used primarily to route power and signalling between the motherboard and silicon, and to protect the silicon. There have been several evolutions (wire bond and lead frame packages, flip chip technology, multi-chip packages), which have increased the number of connections and have allowed Moore's Law further scaling. **Advanced packaging techniques such as 2D and 3D stacking will allow even more transistors per device**. Embedded multi-die interconnect bridge (EMIB) technology allows the use of silicon from different process nodes in the same package, allowing a designer to choose the best process node for that specific IP.

Through the combination of new device technologies, advanced UV lithography and 2.5D-3D packaging, **it is expected that packages with up to 1 Trillion transistors will be possible by 2030.**

Continuous innovation is needed in transistor design, process technologies, lithography and 2.5D-3D packaging to meet the application needs of future devices.

6.2 Device Architectures Tailored for AI

Semiconductors designed to perform AI tasks - AI Chips - are expected to constitute an important market in coming years and companies are **developing specific architectures optimised for AI tasks**. These include AI accelerators and architectures that improve data performance in and out of memory.

Machine Learning algorithms use large data sets to learn and improve. Deep Learning approaches require less data pre-processing by humans. In this area, specialised devices are being developed that allow transfer of large data sets through memory and storage.

Currently, central processing units (CPUs) and accelerators, e.g. graphics-processing units (GPUs), field programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs) can be used, each with different characteristics and efficiency for different use-cases (see 5.2).

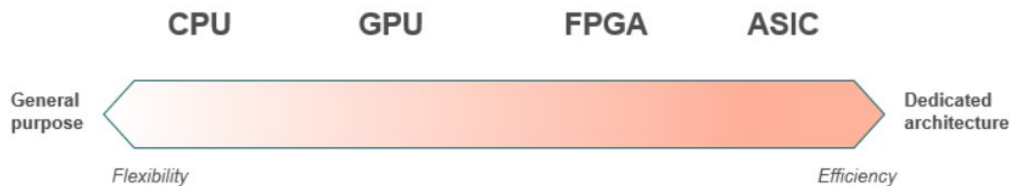

Figure 37. Different types of chips for AI applications

A key need for AI applications **is high bandwidth memory** as the computing layers within deep neural networks must pass input data to thousands of cores as quickly as possible. High bandwidth memory is needed to store input data, weigh model parameters, and perform other functions during both inference and training. This is driving the development of 3D stack of memory that allows Deep Learning to get very fast access to high bandwidth memory.

According to Prof. John Hennessy (Turing Award, chair of Alphabet Inc.), in order to compensate for the slowdown of Moore's Law, **the trend in semiconductors is moving from general-purpose to Domain-Specific Architecture**s: "*the next decade will see a Cambrian explosion of novel architectures, with rapid improvements in terms of performance, as well as in cost, energy and security*". Research is being undertaken in the field. We could group research efforts in microelectronics technologies for AI in the following categories:

- **Massive parallelization** in digital designs: to accelerate matrix operations of deep neural networks;
- **Reduced-precision** acceleration: to speed up computation for deep neural networks, just preserving the needed accuracy;
- **Heterogeneous integration:** Transferring data is a limitation to speed and is power-hungry. Near-memory computing aims at bringing data and processing physically closer; one solution is stacking memory and logic with 3D integration.
- **In-memory computing** performing compute functions in memory to gain speed and power efficiency.
- **Analogue AI** devices: Analogue computing can lead to more "explainable AI" than digital systems mostly operating as black boxes. It can be faster, much more energy-efficient and more "explainable" than digital approaches.
- **Neuromorphic computing** is also called "brain-inspired" computing as it mimics neuro-biological architectures. Its implementation with analogue and in-memory computing can lead to high energy efficiency (100 to 1000 times), making it extremely suitable for Edge AI applications.
- **Photonics AI** is a new research field that aims to mix electronics with optical elements to decrease power and latency in deep neural networks. Silicon photonic chips can exploit optical propagation, and their integration in image sensing devices can lead to ground-breaking efficiency.

New domain-specific architectures, including ASICs and novel semiconductor technologies, will be driving the implementation of neural networks in the booming market of AI chips.

6.3 Open-Source Hardware - RISC-V

The increasing adoption of open source is disruptive as it drastically lowers the barrier to design. China, the US and India, among others, are already investing heavily in open source hardware and software and in order to develop a competitive advantage in key sectors, Europe should support the development of a collaborative ecosystem in this field. The open-source hardware ecosystem is wide ranging and diverse including the semiconductor industry, verticals and system integrators, SMEs, service providers, design tools providers, open-source communities, academics and research.

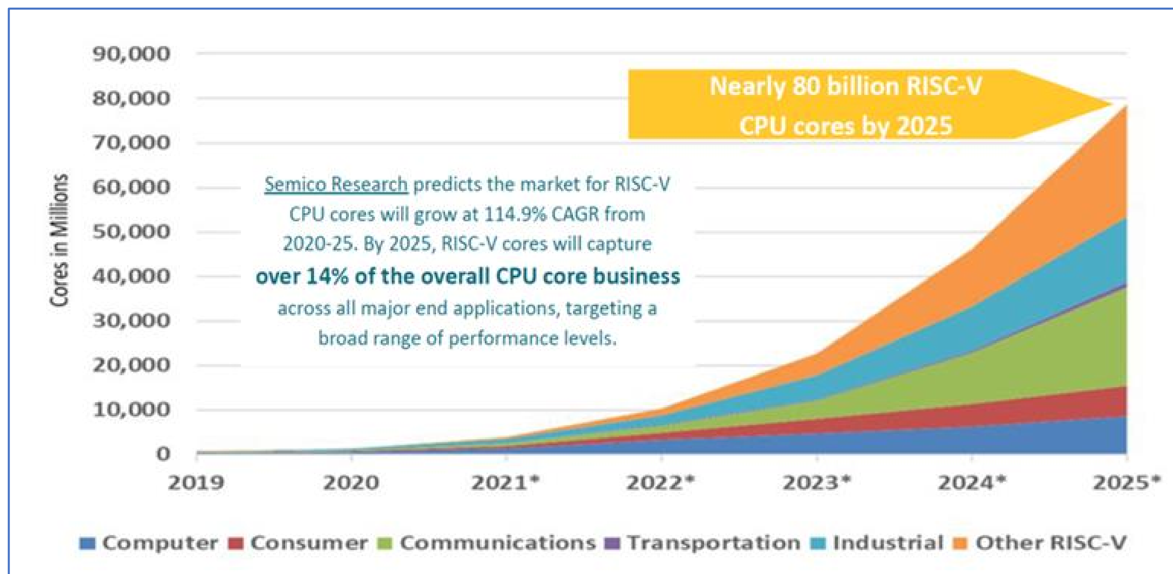

Figure 38. Predicted Growth in RISC-V Market[3]

The predicted growth in the open-source RISC-V[4] CPU market is shown in Figure 38. The benefits and attraction of adoption of open source depends on the type of actor and their role within the value chain. These can include:

- Creating innovative products with lower costs and access barriers.
- Providing a faster path to innovation and smoother cooperation between actors (academic, research, industry, SME, alliances) as no Non-Disclosure Agreement (NDA) and commercial license need to be negotiated.
- Influencing technical choices and specifications.
- Allowing customization of open-source IP to user needs, delivering differentiating products.
- Sharing development costs.
- Reducing risks related to third-party IP (unbalanced commercial relationship, end of maintenance/ discontinued products, export control and trade wars).
- Building support and design service businesses based on open-source IP (such as RedHat).
- Better auditing of security and safety, ensuring that solutions can be fully audited and checked/verified (e.g. possibility to look for back doors in open source IPs). This is not possible for IPs licensed from 3rd parties.

[3] Semico Research Corp., March 2021

[4] RISC-V is an open standard instruction set architecture (ISA) for microprocessors, based on established reduced instruction set computer (RISC) principles, which is provided under "open-source" license (no use fees).

Key areas of interest in the domain are the development of RISC-V compliant processors and accelerators targeting machine learning and cryptography, as well as high-performance storage and communications applications. The use of extended instruction sets to enable more parallel processing, such as RISC-V "P" for Single Input Multiple Data (SIMD) processing and RISC-V "V" for full-scale vector processing, can provide significant performance and/or efficiency gains. However, even higher gains are achievable in many cases by adding application domain-specific features to a hardware architecture.

6.4 EDA Tools and Ecosystem

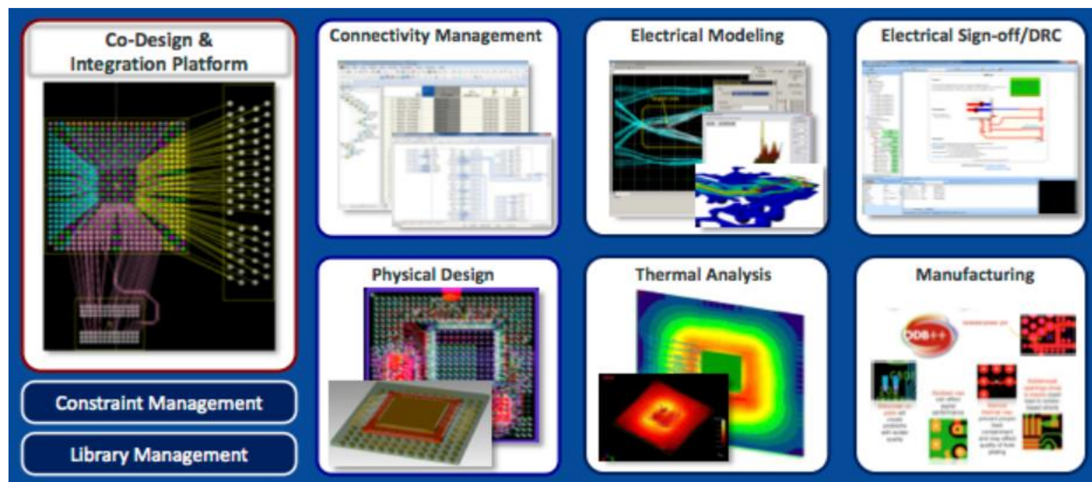

Figure 39. Xpedition Package Integrator Suite (Source: Siemens)

Chip designs can contain tens of millions of logic gates (standard cells) and thousands of memory blocks (macroblocks) made up from billions of transistors, all carefully placed and interconnected by several kilometres of wiring. The placement of these cells and blocks on the chip is critical to the functionality, speed, power consumed and cost of the chip. Electronic Design Automation (EDA) is thus essential for chip design helping designers simulate functionality, integrate IP, optimise floorplan and verify designs. Foundries are also dependent on EDA tools, particularly when presenting coded versions of their manufacturing processes (design rules checks) to design houses to ensure manufacturable chip layouts and reduction of prototyping cycles in design-technology co-optimization. Given the increasingly complex chip design requirements for high performance computing, 5G, AI/ML, IoT, and edge computing capabilities, EDA companies have been prolific acquirers of smaller IP houses to provide integrated, synergistic IP solutions along with their EDA software, becoming significant semiconductor IP houses in their own right. Examples of this are Cadence, Synopsys and Mentor Graphics. A challenge is that the US controls 70% of the global market for EDA tools. However, with the acquisition of Mentor Graphics, Siemens has now become a major player. This offers the opportunity to link and join forces with the European EDA community to collaborate on activities to support European growth in a sector where Europe has very poor presence[5]. The top EDA companies spend more than US$ 1billion annually on R&D costs to continue innovating, so to provide meaningful progress continued investment from the public sector and cross-border collaboration are needed.

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[5] European chipmakers using US-origin IP have to apply for licences to export to China. See chapter 3

As the commercial vendors mostly provide closed source tools, there a move can be observed towards open source tools to support specific parts of the design flow. **Open source tools are essential for introducing new companies and more developers into the field, especially developers with a software background who can bring in innovation in hardware-software co-design**. Developers can freely work together across teams and organizations using massive collaboration hubs such as GitHub or GitLab.

Smaller companies and research organizations need access to professional EDA tools which the large EDA vendors provide through a variety of business models (Cloud offering, specific terms for start-up, research licenses, Software as a Service (SaaS), etc.). The European Commission has proposed to invest in a European open source EDA tooling ecosystem, encouraging open interchange formats and making sure current tools do not introduce restrictions on utilization of open source hardware designs. EDA tools can be exploited in various parts of the development chain including lifecycle management, architecture exploration, design and implementation as well as verification and validation. A key area for the future is in creating transparent, auditable processes for ensuring safety.

By focusing EU investment on tool development and interoperability standards, a mixture of open and closed ASIC tools can be used by designers for future designs supporting RISC-V and chiplet development.

6.5 More than Moore

Moore's Law[6] has driven mainstream microelectronics for several decades resulting in ICs with transistor dimensions at 45 nm and below. While this supports memories and microprocessors, interfacing with the analogue physical world does not scale in the same way. **Radio frequency (RF) devices, power management subsystems, passive components, biochips, sensors, actuators, LEDs, lasers, photonic integrated circuits, microelectromechanical systems (MEMS[7]) now also play an important role in today's semiconductor products.** There is thus a need to integrate analogue functions into CMOS technologies to add value. These devices are called "More than Moore" devices.

The main technical challenges with More Than Moore devices is that they may require unique structures and different materials to those traditionally used. In many cases devices can be fabricated using tools and processes originally developed for older, larger nodes. However, enhancements may be needed with new processes and materials to be deposited and etched. One key challenge is the need for tighter dimensional control. Notably analogue circuits do not benefit from small geometries. Slight variations in one component can have unexpected consequences throughout the circuit which makes them very challenging to design and produce. Providing and managing power is an essential requirement for every device. To do this, some devices are designed with thin vertical structures with large lateral dimensions and some exploit wide band-gap semiconductors like gallium nitride and silicon carbide. There is a need for advanced design technologies to address the challenges of modelling and simulation of reliability, degradation effects and process variability. There is also a need to develop smart fabrication, fab automation and data processing to generate a smart infrastructure. Wafer bonding is a key enabling process technology. There are many applications in low-power devices including energy harvesting, low-power energy conversion and management.

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[6] The number of transistors on a chip doubles every 18 to 24 months
[7] https://www.businesswire.com/news/home/20180809005360/en/

The long-term progression of Moore's Law requires overcoming the exponential growth in the power consumption requirements of current CMOS-based computing[7]. To continue this and create ultra-low power solutions, it is necessary to exploit the quantum effects in materials. This needs to be achieved at ambient room temperatures.

6.6 Quantum Technologies

Quantum Technology (QT) is set to have a substantial impact on the European Union's core industries, including pharmaceuticals, chemicals, and automotive (see Figure 40). **The total combined market for QT at the end of 2021 is EUR 1.7 billion. This is expected to rise to EUR 10 billion in a technologically conservative scenario, and to EUR 89 billion by 2040 in an aggressive disruption scenario**.[8] Overall the effect of QT on the entire economy will be very significant. It could, for instance, transform the ways we develop new drugs, perform medical imaging exams, find optimal portfolios, discover new materials, or the way we communicate securely. These technologies could disrupt the business models of leading players today, giving rise to a range of new products and business models.

Quantum chips are devices that process quantum information, that is, information at the level of individual quantum systems. The level of integration of components onto a single chip varies depending on the technology used. These quantum chips can be used for different applications across the four Quantum Technology pillars that are quantum computing, quantum simulation, quantum communication and quantum sensing and metrology. Standard chips are mainly used in computing machines, but their number is steadily increasing in networks for communication purposes. Similarly, quantum chips are used in computing machines (either as stand-alone quantum computers or accelerators for supercomputers) or in networks where they can provide entirely new services like ultra-secure communications or ultra-precise time. Advances at PASQAL[9], Alpine Quantum Technologies[10], Alice&Bob[11] or IQM[12] , indicate that quantum machines with incredible power are becoming within reach and could be used for rewriting encryptions or accelerating research in numerous industries, including the pharmaceutical industry, material science, logistics, and finance. Such quantum machines are going to be deployed in the market soon and the quantum advantage demonstrated by some of them will soon translate into an industrial advantage as new algorithms are developed and the integration within HPC environment progresses. Quantum chips are also concerned sensors where both low-end (large volumes and cheap) and high-end (low volume and very expensive) quantum sensors need to be pushed toward industrialisation. Quantum communication devices represent another application of quantum chips allowing highly secure communication.

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[8] The Rise of Quantum Computing | McKinsey & Company Excludes internal investment by major technology companies such as IBM and Google.

[9] Pasqal Quantum Computers Coming to Azure Quantum (hpcwire.com)

[10] Compact quantum computer for server centers: Researchers build smallest quantum computer yet based on industry standards -- ScienceDaily

[11] Alice&Bob, a quantum computing startup, raises $30M to launch its first fault-tolerant 'cat qubit' computers in 2023 | TechCrunch

[12] European quantum computing startup takes its funding to €32M with fresh raise | TechCrunch

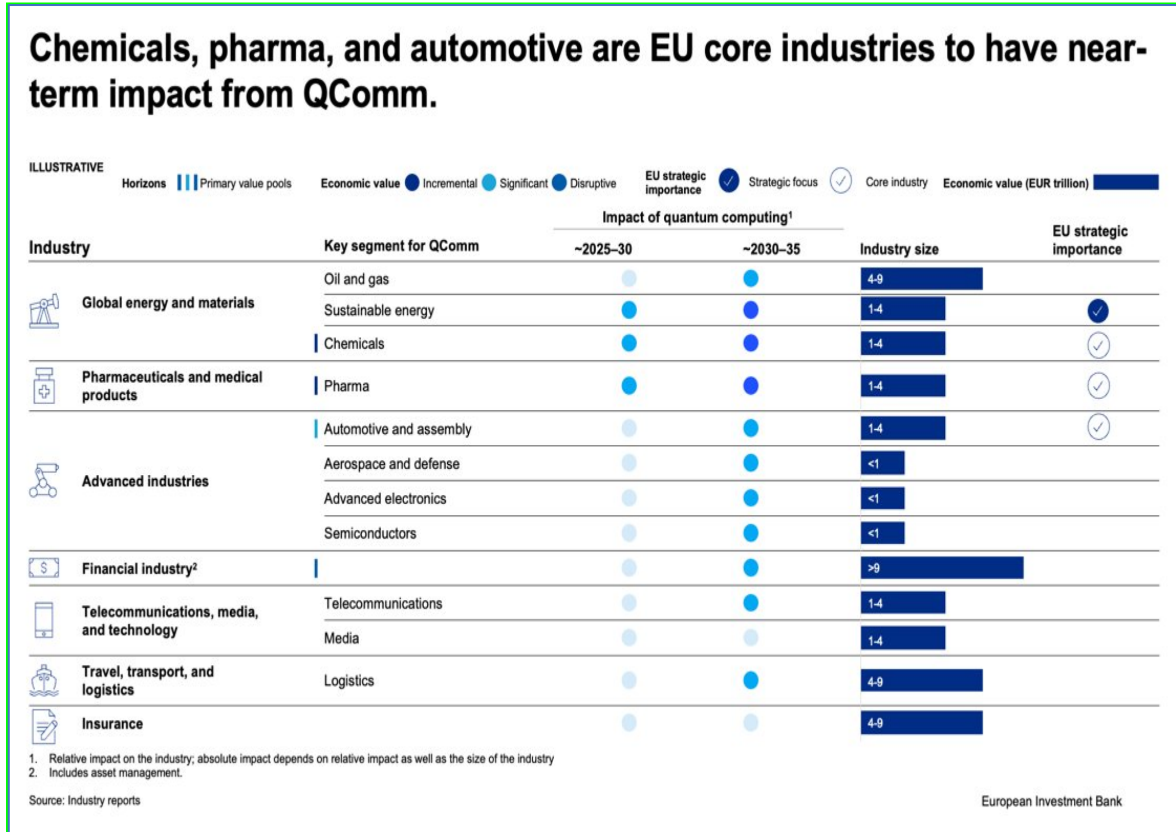

Figure 40. Potential Quantum Technology Markets in EU

In 2018, the European Commission launched the Quantum Flagship, a ten-year initiative with a budget of one billion euros. The European Union, that is, the European Commission and Member States, have also announced EUR 6.1 billion of government funding over the next seven years.[13] The aim is to build on European scientific excellence in quantum and bring research results closer to industrial exploitation and real-life applications, fuelling innovation. Europe has established a climate for QTs that has enabled the number of EU start-ups to grow at a faster rate than in other countries. However, according to a study from the EIB group, these QT start-ups are unable to raise sufficient private Venture Capital funding in Europe[14]: as of the middle of 2021, **around 25 percent of QT companies globally are based in the EU, yet the region has received less than 5 percent of global funding.** Particularly the development of hardware components for QT is capital intensive, and EU deep-tech start-ups in this sector need further dedicated support to attract private investors and bring their innovation to the market.

[13] Some Member States have already established large national quantum programs, notably France (EUR 1.8 billion), Germany (EUR 2 billion) and The Netherlands (EUR 0.65 billion), with complementary objectives and activities such as the knowledge transfer from the research labs to industrialisation, supporting the emergence of a European quantum industry, including design and production capabilities of quantum chips.

[14] “Financing a quantum technologies industry in Europe”, McKinsey, EIB, 2022

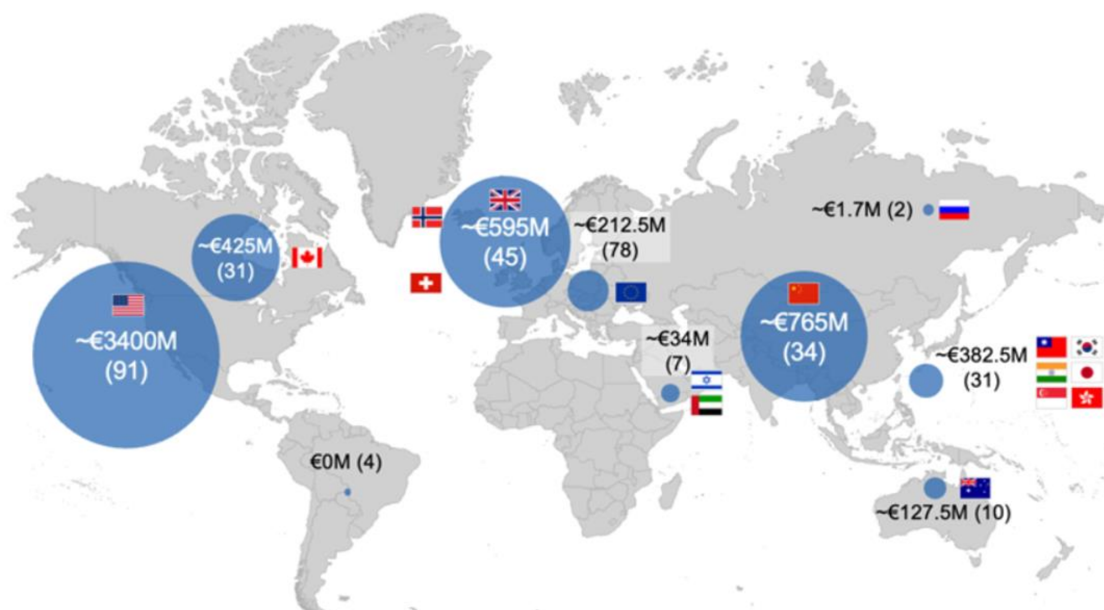

Figure 41. Funding (and number) of QT players by region. Sources: EIB, McKinsey,

The most critical parts are control electronics (possibly cryogenic control electronics), connectivity, and I/O (especially measurements). Despite not being part of quantum chips per se, these components are key to the development of QT (particularly for superconducting and solid-state qubit platforms and single-photon detectors based on superconductors). Importantly, the production of cryogenic control electronics may require specific equipment in the fab facilities. **Quantum chip innovators also need access to dedicated clean rooms and foundries for prototyping and production.** Currently, some European quantum chip innovators are obliged to make use of US facilities, as they do not have access to the relevant facilities in Europe[15].

Europe is a leader in Quantum Technology research. In order to turn research investments into market innovations, quantum devices need to be fabricated. Quantum chips need specialised facilities and if Europe does not invest, key innovations will either fail to reach the market or will go abroad for financing.

[15] Second workshop on Quantum Chip Act organised by the EC with participation of academia, RTOs and Industry representatives, 19 October 2021.

PART II - A Plan for Action

7. The Chips Act: the way forward

As mentioned in **Chapter 1**, the production of chips relies on collaboration and trade between the major semiconductor-producing regions. Complex interdependencies across the value chain and many potential choke points, stemming from concentration of essential technologies or activities within particular companies or geographies (more than 70% of foundry services are in Asia, for example), makes it prone to disruption. As illustrated in Chapter 1, failures or shortages at any point in the value chain can have repercussions across the full supply chain.

These structural weaknesses coupled with lean production strategies and geopolitical tensions, which had interrupted established trade flows even before the pandemic, left the industry unable to cope with the surge in demand following the onset of the pandemic. The impact of the ensuing shortage on the European economy has been severe. As set out in **Chapter 2**, automakers are still having to wait for periods of up to a year or more for chips; many have had to reduce production or shut down, laying off workers.

Many other sectors have been impacted by the shortage, which has brought to light the degree to which semiconductors have penetrated every facet of society. Yet they will continue to find increasing use; the market for semiconductor chips is expected to double between 2020 and 2030 to a value of more than USD 1 trillion.

However, as shown in **Chapter 3**, the level of consumption of semiconductor components in Europe is much higher than (around twice) the value of components produced in the EU or even the value of components produced by European companies globally. In 2021, the EU's trade deficit for semiconductors was almost EUR 20 billion with exports amounting to EUR 31.5 billion while imports amounted to EUR 51 billion. And in 2021, fabs were operating at full capacity.

The EU has observed in the last 20 years a gradually declining share of global manufacturing capacity. Moreover, roughly 50% of capacity in the EU is concentrated at nodes of 180 nm and above. Design competences are largely concentrated on analogue, power, microcontrollers and MEMS - important for systems operating in the real world; for processors and memory components - central to computing - competences are scattered and confined to niche applications. This is reflected in industrial research efforts which have focussed on the former, rather than equipping the Union for digital transition (see also section 3.3.3).

These are major concerns in light of the fact that future market growth is forecast to be concentrated below 10 nm nodes, where chips are needed to process ever-higher volumes of data, perform at higher speed and with less energy consumption. Application domains where the EU needs to maintain and build resilience - automotive, industrial automation, communications, aerospace, defence and security - will on the one hand continue to rely on many types of analogue, power, microcontrollers and MEMS components, and on the other make use of leading-edge processors (10 nm and below) to perform tasks autonomously as presented in **Chapter 4**. Chapter 4 also points to needs in advanced packaging/ heterogeneous integration, wafers and materials for power electronics and communications, and a more assertive approach in standards (healthcare, automotive, communications and security).

By leveraging existing industrial strengths in security and its lead in R&D on new computing paradigms that enhance computational power and drastically reduce energy consumption, the EU has a real opportunity to capture market shares in strategic emerging technologies such as edge-computing

and AI. As set out in **Chapter 5**, edge computing and AI will be widely deployed i.a. in automotive and industrial market segments where the EU's strengths in system design lie; sustainability and security will be key differentiators in these and many other future markets.

However, leading technology companies in other regions are making large investments in squeezing more transistors into ever smaller volumes of silicon, in a race to master next generation technologies such as GAAFET and RibbonFET, and advanced packaging techniques such as 3D stacking and chiplets. These companies are also active in exploring new device architectures for AI and quantum technologies. Europe is at the cutting-edge of R&D in these domains; with the possible exception of ASML however, there are few European industries actively exploiting the fruits of such R&D efforts as shown in **Chapters 3 and 6**.

Open-source approaches and open platforms can reduce dependencies on a limited number of suplliers and European companies are attempting to make strides in design with open hardware platforms to generate IP for accelerators and processors, and open source EDA tools. However more can be done, for example in advanced packaging.

In terms of technology capacity, the EU clearly has strengths that it can build on, but has serious gaps which if not addressed could even lead to current strengths being eroded.

It is against this backdrop that the European Commission presented the Chips Act package, with measures and actions to address the weaknesses outlined above. These weakness can be grouped under the following 3 headings with the three foundational pillars in response - further elaborated in **Chapter 8**:

Limited innovation capacity in the ecosystem

- The EU's research programmes have largely not driven **the conversion of its excellent research results into industrial innovation**. They have fallen short in stimulating the partnerships at industrial (end-user) level that would exploit such developments and in playing a leading role when it comes to driving new trends, platforms and standards.
    - For example, the EU has pure play foundries as well as IDMs with in-house production facilities and some few companies active in back-end manufacturing. While these companies perform well in specific market segments, many of the world-leading innovations developed by the EU's RTOs and are taken up in other parts of the world. Consequently they have not led to diversifying and strengthening the EU's manufacturing base, in particular as regards digital technologies and leading-edge nodes.
    - **Similarly, while the EU has important strengths in systems design, it has significant weaknesses in digital design** and in particular in processors. As explained in section 3.3.3, this can in part be attributed to a focus by companies on core business, even when it comes to investing in R&D. Furthermore, EU systems houses (end-user companies) have been less present in research activities focussed on semiconductors, which limits the diversity of efforts by suppliers and is a missed opportunity to strengthen user-supplier relations which can stimulate transfer of results into innovation.
- **SMEs and start-ups have difficulty attracting the necessary investment** to develop their ideas and scale. This has led to stagnating growth of an indigenous European ecosystem and ultimately

creating gaps at the cutting-edge of technology. Specifically, the EU's footprint in the fast growing fabless design segment has declined to less than 1%[16]. mergr

- **As the EU industry has pointed out in a report published in 2018,**[17] the EU has a limited pool of talent, and lacks a workforce with the necessary skills.

To address the above, **Pillar 1 of the Chips Act, the Chips for Europe Initiative**, will create an ecosystem to build up coordinated R&D efforts and technological capacity at scale throughout the Union. Through the set-up of large scale-pilots and a virtual design platform – that are designed in consultation with industry – to ease and accelerate the testing and validation of new concepts, and their transition to commercially viable products, it will provide conditions for European industry to create and deploy cutting-edge technologies to capitalise on the opportunities ahead in domains such as AI and edge-computing, and supply the needs of key sectors (such as automotive, industrial automation, communications, healthcare). Through a network of competence centres it will facilitate access to these facilities by stakeholders across the Union and will further develop the diverse initiatives on skills. It will also deploy a Chips Fund with the aim of facilitating further growth in particular of smaller innovative companies active in design and integration.

With the exception of the Chips Fund, the above activities will be implemented under the Chips JU which will replace the KDT JU. To assure its strategic alignment with the goal of strengthening Europe's semiconductor ecosystem, the EU and national authorities will outline the work programme – taking into account advice from relevant stakeholders.

Low investment in manufacturing capacity

- The EU depends excessively on production capacities located in third countries - it is a net importer of semiconductors, particularly for the most advanced ones at the leading edge – in fact, it has no foundries for nodes smaller than 22 nm.
- The EU also depends on third countries for certain types of wafers such as SiC and GaN, the availability of which will be crucial for further innovation in the automotive, communications and energy sectors, and for the realisation of EU's green transition (see sections 4.2, 4.4 and 4.6).
- The shortage has served to highlight vulnerabilities throughout the **entire** supply chain. EU-headquartered (and other) companies face difficulties in acquiring microcontrollers, analogue, opto-electronic and other chips including those for which the EU has fabrication facilities and despite their running at full capacity.
- Given the continued increase in demand for semiconductors, companies needing smaller volumes of specialised chips are particularly hit by the crisis, including those who produce equipment needed for chip-manufacturing[18].
- There have been bottlenecks due to packaging being concentrated in South East Asia where problems with transport and logistics continue to persist (see section 2.6). Shortages of materials also slow production and can bring it to a halt.

[16] Sales growth of fabless companies in 2020 is 24%, compared to 8% for IDM companies. Source: IC Insights/McClean report 2021.
[17] Boosting Electronics Value Chains in Europe, June 19, 2018
[18] Chipping In For Equipment Suppliers: The Equipment Multiplier Effect On The Chip Shortage, Semiconductor Engineering, May 2022

- Currently, less than 4% of global CAPEX investments by the sector are made by EU headquartered companies. The ever-increasing costs and complexity of establishing production capacities mean that investments can be highly risky; furthermore there are long lead times before investments translate to increased capacity.

To address the above, **Pillar 2 of the Chips Act, Security of Supply**, proposes to make use of a framework that contributes to the security of supply and that can help to strengthen the resilience of the semiconductor ecosystem in the EU, by fostering investment in first-of-a-kind facilities which should be beneficial for the entire semiconductor ecosystem in Europe. These can, moreover, be expressly mobilized for critical sectors or important economic sectors in Europe in times of crisis.

Imbalance between supply and demand

- Disruptions in the supply of semiconductors have very negative effects on Europe's economy and society. The complexity of the semiconductor supply chain makes it difficult to identify and assess risks related to potential shortages and take the appropriate mitigating action. This will require more transparency together with more detailed information to be provided regularly by industrial stakeholders.
- In response to shortages, some Member States (MS) have announced their intention to take unilateral action to be able to anticipate and mitigate possible disruptions, as cooperation on effective, coherent actions is lacking at EU level.
- There is a lack of a coordination mechanism between MS and the Commission as well as among MS themselves with relation to efforts in the field of semiconductors.
- In the toolbox of the Commission and of the MS, there is a lack of effective instruments that may help addressing potential shortages.

In response, **Pillar 3, Monitoring and Crisis Response**, will establish a coordination mechanism between the Member States and the Commission to better anticipate and mitigate the effects of shortages. It includes a monitoring scheme and a crisis mechanism with a dedicated toolbox of measures that can be triggered in the event of a crisis.

Why this proposed course of Action?

On 23 May 2013, the European Commission announced An Electronics Strategy for Europe[19], with the objective to reverse the declining European share of the world market, and to ensure that Europe makes the best of semiconductor technology to boost innovation, growth and jobs creation across the economy.

Specific targets were, by 2020, to facilitate industry investment of €100 billion; double the value of EU micro-chip production; and create 250 000 jobs in Europe. The strategy was implemented primarily by means of the ECSEL JU and by making use of the IPCEI instrument. The latter was initiated in recognition of the fact that a new qualitative and quantitative approach was needed in order to allow industry to invest again in Europe as is done in the rest of the world. The IPCEI requires innovation to be beyond the global state-of-the-art which limits its utility. Nevertheless both initiatives served to unleash investment in Europe (see section 3.3.3). However, the concrete targets

[19] 'Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions — A European Strategy for Micro- and Nanoelectronic Components and Systems' COM(2013) 298 final

have not been met – in particular the EU's share of production is declining as investment in other parts of the world continues to increase. There are several reasons for this, notably:

- The agenda for R&I has been very much industry driven[20] and therefore largely focussed on shorter-term core business interests; policy-makers (the Union and Participating national authorities) did not have the possibility to be proactive in driving investment in longer term strategic targets.

- Despite the emphasis given to the importance of involving demand-side industries, their participation was very limited.

- The EU potential to design chips was given insufficient attention.

- While the sector was confronted by increasing geopolitical tensions - driven inter alia by intense competition between the US and China[21]; technological and economic challenges - as miniaturisation becomes ever more complex and costly; use of subsidies[22] which distorted the playing field; the EU was equipped with limited means to respond.

- The lack of an over-arching framework to monitor progress towards the targets meant there was little drive or impetus at EU level, and limited awareness of the strategic importance of the sector.

- Action around skills and investment funds were part of the 2013 strategy, however microelectronics was bundled with other so-called Key Enabling Technologies, and follow-up specific to the sector was minimal.

- Despite the Union having agreed to an increase in the budget of the KDT JU, relative to its predecessor, for the 2021-28 Multiannual Financial Framework, the lack of shortages did not create the necessary political momentum for policy makers in all countries to embrace the initiative through new instruments.

The shortages of semiconductors have been an instigator of change. It has raised awareness at all levels of society of the critical role of semiconductors for the economy. The Chips Act represents a holistic response to the shortage bringing: increased funding to support research and capacity building and new mechanisms for implementation; a driving role for the Union and Member States – in consultation with industry - for defining areas of strategic interest; more focus on harnessing Europe's chip design capability; dedicated activities on skills and investment funds; new concepts, such as "first-of-a-kind facility in the Union" for establishing security of supply; and mechanisms to define indicators to understand the state of the industry, monitor the supply chain and to mitigate the effects of crisis.

This represents a step change from the past.

Coordination across all three pillars of the Chips Act will be of the utmost importance therefore to ensure coherence, effectiveness and efficiency of implementation. Given the existence of bodies such as the governing boards linked to the current KDT JU and the Alliance on Semiconductors and Processor Technologies, and the need for a coordination mechanism for the implementation of Pillar

[20] Interim evaluation of the ECSEL JU
[21] With the announcement in 2015 by China of its Made in China Initiative
[22] Measuring distortions in international markets: The semiconductor value chain, OECD December 2019

3, a clear Governance structure will need to be put in place, to define the roles of and interactions between participatory bodies, and to drive and monitor progress.

Subsequent to agreement by Member States on the KDT JU, an IPCEI with substantial participation from Member States and industry has been pre-notified to the Commission. This represents a positive EU-wide effort to mobilise resources towards strengthening the European ecosystem.

8. The Three Pillars of the Chips Act Package

8.1 Pillar 1. The Chips for Europe Initiative

8.1.1 Introduction

As discussed above, Europe's research programmes were not designed to bridge the gap to production, and hence have not translated its excellent research results into industrial excellence and market breakthroughs. In contrast, investments in Europe have tended to be focused on particular technologies such as power electronics, RF and analogue for specific applications, but generally not in mainstream digital technologies.

Industry, with support from Member States, has of late begun to step up on investments in both R&D&I and First Industrial Deployment. 19 Member States have recently pre-notified a second[23] Important Project of Common European Interest (IPCEI) to the Commission, with more than 100 industrial participants (up from 32 in the first IPCEI). In terms of technologies and application domains this goes beyond the first IPCEI in putting for example also communications as a major focus; it addresses R&D&I and First Industrial Deployment of a range of advanced microelectronic technologies and supports their application in downstream industries. The proposed IPCEI has mobilised a large number of SMEs from across the Union and has served to raise widespread awareness of the Union's efforts to promote investment in semiconductor technologies.

This is a positive development, but a more coherent response is needed to address the set of problems outlined in Chapter 7 and the preceding chapters above. Europe needs to establish and invest in an infrastructure to develop knowledge and expertise in building technologies such as processors as well as new emerging technologies such as AI, neuromorphic, quantum etc. It also needs new semiconductor production nodes below 10 nm to satisfy upcoming market needs, as explained in Chapters 1-6. Building this expertise and capacity in Europe at an industrial level is essential for Europe to stay at the forefront of innovation; the only way to achieve this is to invest in new infrastructures in design platforms and pilot lines as outlined below.

8.1.2 Explaining further the Pillar 1 approach

The Chips for Europe Initiative (Pillar 1 of the Chips Act package) was designed to address the research, development, and infrastructural gaps in Europe. It aims to invest in activities that would **close the gap from lab to fab**, by

i) **Leveraging European strengths** – starting with existing capacities and research expertise
ii) Further **reinforcing technology capacities** – which implies addressing the gaps and preparing for longer-term capabilities.

[23] Details of the first IPCEI are provided in Ch 3.

That will only work through a **collective effort by all stakeholders**: EU and Member States across the Union; industrial actors across the full value chain; researchers and RTOs. A concerted set of activities would start with **design** that has to date been a weakness in Europe, which is also reflected in the lack of indigenous fabless companies. A good base in design capabilities is needed to feed into the rest of the innovation value chain and prepare for the necessary components, systems and ultimately products to be developed and produced in Europe.

To this end the **Chips for Europe Initiative** proposed to set up:

- **A (virtual) design platform accessible across the EU** offering Electronic Design Automation (EDA) tools , IP libraries (created and combined by RTOs and participants across the EU) and integrating and standardising libraries from **existing pilot lines** (see Annex 5). The idea is to provide user-friendly routes to design of new functionalities or new chips and systems for innovative SMEs, IDMs, fabless design companies and vertical industries.

- **Pilot lines that are open for research, testing, experimentation and validation** of new device concepts. The idea is to start with existing pilot lines (e.g. from the ECSEL JU) and **bring them to a higher level of maturity** to facilitate research, development, test, experimentation and validation of these novel technologies by industry in their designs. By carrying out research on the pilot lines, the whole innovation cycle will be accelerated.

Europe needs to catch up in its innovation capabilities in design and development as quickly as possible. The best way to achieve this is to develop a design platform that will use the existing capacities and infrastructures in a way that will help industry shorten its design and development cycle. This will be done by creating **a virtual platform**, providing users with Electronic Design Automation (EDA) tools and integrating libraries from **existing pilot lines** (see Annex 5) that can be used for designing new functionalities or new chips and systems. This would all be networked together and made widely available in Europe, creating a large capability with potential innovations in all relevant technologies such as FDSOI, FinFET, heterogeneous integration, and silicon photonics, but also others for particular applications. Starting in this way with existing pilot lines now will enable production in the respective technologies in **2024-2026**. At the same time, it is essential to set up **new pilot lines** to create capacities where the EU has gaps, notably in design and production at advanced nodes, by **2027-28 and beyond**.

8.1.3 Investing in a pan European virtual design platform

The design platform will be **available to users across Europe**. It will be continuously upgraded with new design capabilities. In this way it will stimulate a wide cooperation of users' communities with design houses, IP and tool suppliers, designers and RTOs, and cater for the design of novel components and systems for multiple applications such as low energy, security, system integration and 3D assembly. To exploit synergies across pilot lines, design elements specific to each pilot line will be integrated in a broader design environment providing designers with a common structure that is more efficient and richer in technology options.

The **design platform** will also provide for creation of **virtual prototypes** based on technology that does not yet exist physically. This would in turn allow different integration technologies and manufacturing options to be explored. Such early insight will boost the European design ecosystem for the advanced nodes, allowing for example to examine the impact of various design options on the cost, sustainability aspects, and overall performance of the device. This virtual prototyping can further

shorten the product development cycle and reduce time to market, thereby increasing the users' competitive edge and leading to cost savings.

The design platform and pilot lines should **operate in a synergistic way** – after virtual prototyping, device designs can be implemented on the pilot lines; the resulting specifications and performances will feed back to designers who can then refine and improve the design models before the next prototype stage, a **functional demonstrator**, or its transfer to manufacturing. The complete concept and ecosystem is illustrated in figure 42, below.

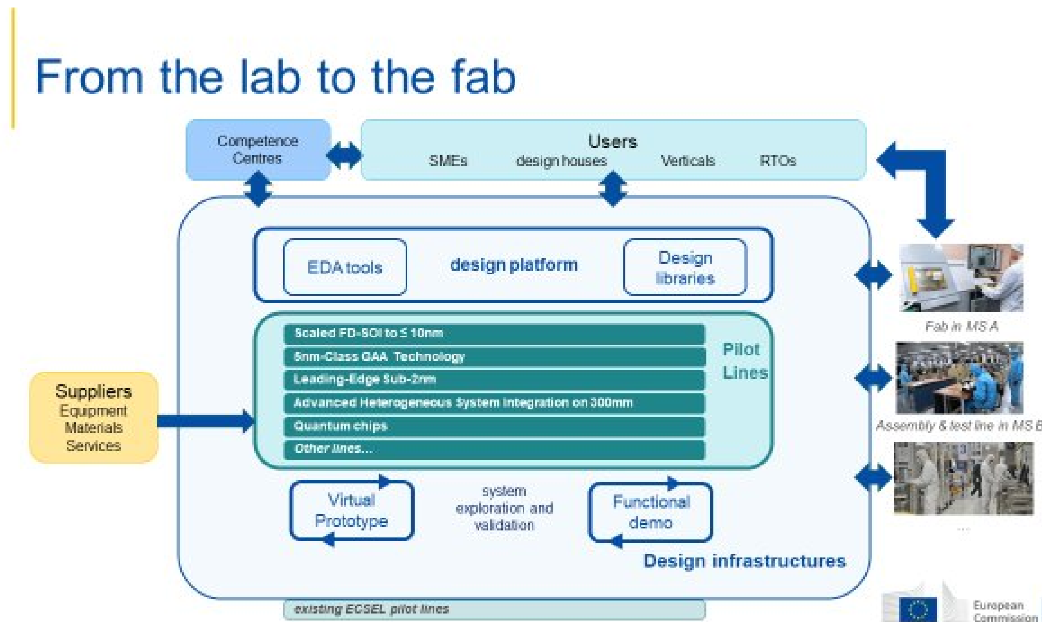

Figure 42. The design infrastructure, pilot lines and relations with users, suppliers and competence centres

Process design kits specific for their technology will be developed by the "owners" of the pilot lines. They can in turn be integrated into EDA tools for use together with libraries of predesigned components to automatically generate the physical layout of new chips. This is a two-way process as issues impacting design are also fed back into the process development to optimize the technology. The availability of these design modules will allow to start chip development cycles even before the full technology is established and ready for yielding production.

Pilot lines allow research to be carried out in an industrial setting but also bring together research activities from various competences, in a way that these bring results that are directly applicable in a production environment. There are currently at least 16 **existing pilot lines** in 10 Member States (see Annex 5). Some of these could be potentially integrated in the design platform infrastructure. The ones addressing the most essential technologies would be integrated first; others could be added according to demand and as the infrastructure is further developed. These were for the most part developed under the ECSEL JU and the Photonics21 public-private partnership[24], and some have already demonstrated technologies from EUV to FinFET and FD-SOI to heterogeneous integration and graphene as well as photonic integrated circuits. Some of these technologies have been taken up by industry and are now on the market.

[24] www.photonics21.org

To date, pilot lines have operated largely separately and independently; by bringing them together in the Chips for Europe Initiative, their complementarities can be exploited in a synergistic way. As mentioned above, process design kits can be developed and reused in new device design as well as libraries that can be shared throughout the design platform.

8.1.4 Investing in competence centres and skills development

A competence centre is a single entity or a coordinated group of entities, with complementary expertise and not-for-profit objectives, capable to support activities in the area of microelectronics and help companies, especially SMEs and small mid-caps, as well as academia, to develop and/or integrate semiconductors in their processes. Competence centres will provide services to facilitate access to pilot lines and to the design platform, provide training and skills development, and support to find investors, make use of existing local competencies and reach out to the relevant verticals. The services will be provided on an open, transparent and non-discriminatory basis.

Once the design platform and associated pilot lines have been put in place, **access** to this infrastructure, virtual facilities and services, must be provided. For this, in each Member State design houses and **competence centres** will be set up to provide access to the tools and libraries and to coach people in how to use the new infrastructure. Linking these through a **network** of competence centres will ensure sharing of information, and local access for users to expertise, to the design platform with its tools and libraries, and to the use of the pilot lines on a pan-European level.

Each competence centre will represent an access point to the European network of competence centres in microelectronics, helping local companies and/or academia to get support from other centres in case the needed competences fall outside their area, ensuring that every stakeholder gets the needed support wherever it is available in Europe. Furthermore, they will connect and be part of the European network of competence centres, European Digital Innovation Hubs (EDIHs) or other innovation ecosystems such as Knowledge and Innovation Communities of the European Institute of Innovation and Technology (EIT KICs), acting as a multiplier for the field of semiconductors and widely diffusing the use of all the microelectronics capacities built up under the Chips for Europe Initiative. Typical entities contributing to the centres will be RTOs or university labs offering technology services, which could work in collaboration with partners whose expertise lies in business development and training. Through these national centres, this networked system will offer unique, world-class innovation capacities in design, virtual prototyping, and design refinement to users. Subsequent real prototyping on the physical pilot lines will provide large scale testing and experimentation of the designed chips and systems with greater and more successful commercialisation provided through reduced costs and a faster route to market. Taken together, this infrastructure and toolset will also facilitate developing and improving the performance and capacities of the more mature technology nodes, which will remain important for many large-scale applications.

The Initiative will provide the R&D community, RTOs, suppliers of technology services, industry, SMEs and start-ups across Europe with ready access to the most advanced technology and design infrastructure. This can be organized in various forms - for example, as cooperation projects with specific focus on building and strengthening the network and with a clear business case in mind. Community interface planes will be set up at several levels ranging from system houses, providers of commercial packaging, testing solutions, application industry to regional competence centres, EDIHs, SMEs and start-ups. Goals are (i) to lower the threshold to access the technology of the pilot lines and fabs; and (ii) to accelerate the design process.

One dimension of the support provided by the competence centres will be the provision of **training** and **development of the necessary skills**, not only in the use of the design tools and infrastructures but also more widely in those required to address the severe skills shortages faced by the EU microelectronics sector (according to the European Commission ICT Monitor, the current number of open vacancies for electronics engineers in Europe is 64 000, and according to the European employment database EURES, it is more than 320 000[25]). To address this and in order to grow the European ecosystem to meet the goals of the European Chips Act, it is essential to train a workforce. The "Pact for Skills"[26] announced by the Commission in November 2020 set out a new engagement and governance model for mobilising and incentivising stakeholders to make concrete commitments for upskilling and reskilling. It is estimated that more than 250 000 students and workers (from within the sector and coming from other sectors) will need to be skilled/re-skilled across Europe. The number of open positions for engineers and technicians is growing at an alarming rate[27]. The blistering pace of technology calls for rapidly evolving skills in R&D, design, manufacturing, specific applications, AI ethics, cybersecurity, quantum technologies and energy-efficiency. The Chips for Europe Initiative will contribute to building and strengthening the European microelectronics workforce, including through the competence centres which will actively engage with the complete spectrum of education and training providers, with the companies and with the learners. Horizon Europe programmes on skills development and competencies curricula will be complemented by capacity-building in advanced applied digital skills and competences in semiconductor and quantum technologies supported by the Initiative. Moreover, through the Pact for Skills initiative and the Semiconductors Alliance, the Commission will facilitate closer collaboration between industry and academia and the organisation of internships and apprenticeships.

8.1.5 Investing in new pilot lines

Harnessing the existing pilot lines is only the first step and will deliver results for production around 2024-2026. To this infrastructure would be added **new pilot lines** addressing the most advanced technologies to fill the existing gaps in Europe's technological capability and reach the 2030 ambition of being at the leading edge for advanced production capabilities (see Annex 6). These will be developed as research pilot lines to address specific technology challenges, including test and validation. They will have different characteristics in view of satisfying the user requirements, and maximise the successful transfer of results into the industrial environment. The relative involvement of research organisations and industry will depend on the level of technological maturity addressed.

Examples include:

- **FD-SOI at 10 nm and below.** At 22 nm and as already planned at 18 nm, currently FDSOI is the most advanced technology present in foundries and IDMs in Europe. To support their needs and those of the fabless companies using this technology, research and development of further node scaling is required. Much stronger engagement with system companies should also be established to speed up the introduction of new technologies that have similar fabrication requirements, like imaging, photonics, RF, and power, in various applications like IoT, health, and cybersecurity.

[25] https://ec.europa.eu/eures

[26] EU Pact for Skills: upskilling and reskilling initiative for those training and working in the microelectronics industry | Shaping Europe's digital future (europa.eu)

[27] Nearly 1.1 million job advertisements for electro-engineering workers were placed in the EU between mid-2018 and the end of 2019 (CEDEFOP, 2020).

- **5 nm-Class Gate-All-Around (GAA) Technology for embedded applications.** A full 5 nm-class GAA technology is to be developed with embedded non-volatile memories and compatibility with 3D stacking, suitable for centralised applications in vehicle electronic architectures, edge computing, 5G/6G infrastructure equipment in telecommunications networks, and industrial automation. This will require to exploit the synergy of process modules already pursued by leading-edge nodes like EUV lithography and nanostructured silicon channel integration and will benefit from the research and development efforts on 2 nm leading-edge node GAA technologies.

- **Technology Pilot Line for Leading-Edge Sub-2 nm with a Nanosheet Baseline (<5 nm).** This pilot line will require advanced research and development efforts as it extends beyond existing research line capabilities to deliver modules 'at-pitch' for the next-generation technology nodes as building blocks for the advanced semiconductor roadmap. This will be done in partnership with the semiconductor ecosystem to address Power, Performance, Area, Cost and Environmental impact (PPAC-E) from a system integration point of view, while considering manufacturability and technology insights from the foundries and suppliers. As technology options mature, smooth transfer of know-how will be made in partnership with one or more leading-edge manufacturing partner.

- **Advanced Heterogeneous System Integration Pilot Line on 300mm (AHSI-Pilot Line).** The objective is to offer integration of complex systems (together with R&I, as required) using combinations of different electronic and photonic technologies. This will allow to benefit from the chiplet approach in the industry to integrate advanced semiconductor functionality (manufactured in the most appropriate CMOS technology node). In addition, it will allow to embed new functionalities on chips to enable new sensor applications e.g., for automotive or advanced sensor technologies. Heterogeneous integration of new materials like SiC and GaN will enable very efficient energy conversion (power semiconductors) and wide bandgap semiconductors (SiGe and III/V) will allow very high data rate communication. Additional developments will concern new materials research and engineering for photonic chips and systems.

Although these pilot lines address different technologies, **operating them under a single structure will maximise the synergies between them and bring benefits**: aligning investment in tools and module development; reducing redundancies and improving specialisations in each line; sharing experiences and expertise; providing a single point of contact for prospective users and access to the lines; networked training courses and skills development; and creating a critical mass by bringing together some 10.000 researchers, a portfolio of thousands of patents and high-class cleanrooms.

Other lines may be added in due course. Critical sectors such as Space and Defence may require dedicated pilot lines or priority on pilot lines addressing relevant technologies.

8.1.6 Investing in Advanced Technology and Engineering Capacities for quantum chips

Today, there are no standardised design and manufacturing processes for quantum chips, which are proprietary designs and in essence hand made. For large-scale uptake and mass-market applications, it is necessary to develop such standardised processes. As the underlying materials and structures are in most cases similar to traditional microelectronics or photonics, the design and manufacturing process of quantum chips need to be aligned with those of the traditional semiconductor industry. This would have the additional benefit of facilitating integration of the quantum device with the control

electronics, connectivity, etc., necessary for the quantum devices to work, but now missing and largely external to the quantum chip.

The European Commission has therefore proposed to complement, in the Chips for Europe initiative, the activities it is already financing under Horizon Europe's Quantum Technologies Flagship. The Chips for Europe initiative would thus focus on the specific needs of the future generation of information processing components exploiting non-classical principles, notably chips exploiting quantum effects (i.e. quantum chips) based on research activities, notably by investing on (a) Innovative design libraries for quantum chips; (b) quantum pilot lines; and, (c) testing and experimentation facilities.

- **Innovative design libraries for quantum chips:** The aim is to align the design and fabrication processes of quantum chips with the well-established and standardized processes of the classical semiconductor industry. This should not only accelerate the capability of the Union to mass-manufacture in a reproducible way quantum chips but will also facilitate the integration of the quantum devices as sensors or processors within the classical microchips. This should be complemented by the development of standardised design libraries and fabrication processes for the quantum chips that are not compatible with semiconductors, but are relying for example on nanostructures.

- **Quantum Pilot Lines:** The Quantum Technologies Flagship Initiative, with the support of the RTOs, is establishing the first quantum pilot lines to bring together the different and proprietary quantum chip design and fabrication processes to achieve harmonisation and compatibility with the existing manufacturing infrastructures. This should bring the design and fabrication of quantum components closer to the well-established processes of the classic semiconductor industry, for all semiconductor- and photonics-based qubit platforms. This will lead to a miniaturisation of the quantum chips, and a higher integration density. Under the Chips Act those emerging quantum pilot lines will be integrated with the relevant semiconductor pilot lines in view of further maturation, and to develop the mass-manufacturing capability. It will also address the integration of quantum components as chiplets in semiconductor microchips. For the alternative qubit platforms, that are not compatible with semiconductors, the quantum pilot lines will form part of the advanced pilot lines to be operational by 2026 – 2027.
- **Testing and experimentation facilities:** The pilot lines will also provide access to testing and experimentation facilities where tailor made quantum components can be tested, including the components produced by the pilot lines.

In addition to the above, the semiconductor competence centres will bring together designers, producers and users of quantum components to develop the next generation(s) of quantum devices as stand-alone quantum chips, or as quantum devices integrated in the classical microchips.

8.1.7 Managing the Intellectual Property

As an overall principle, Intellectual Property (IP) rules should maximize the opportunity to enter the market by deploying foreground IP for specific product-market combinations. In this spirit, where needed and feasible, background IP should be made available to other consortia members in order to facilitate the exploitation of foreground IP. With regard to the set-up of pilot lines, general principles will need to be established up-front that allow co-ownership in the cases of co-invention, and shared IP rights when sharing risks and investments.

Process technology IP should enable technology transfer at a later stage. Exclusive IP rights in certain partner-product-market combinations may be warranted, guided by specific conditions - for instance, in the case of exclusive contributions to associated R&D. For example, this can be the case with contributions from the users, and in case of spin-offs, start-ups being generated. The overall aim is to enable open IP platforms in Europe for rapid growth.

These general principles should allow partners to collaborate on R&D challenges and also focus efforts towards developing prototypes. They should also recognize that in breakthrough research phases, more generically applicable results will be achieved that allow for more flexible and broader sharing arrangements than when approaching the prototype phase where application- and partner-confidential information will necessarily apply.

8.1.8 Implementing the Chips for Europe initiative: the Chips Joint Undertaking

The Chips for Europe Initiative as outlined above would be implemented via the Key Digital Technologies Joint Undertaking (KDT JU), which would have its scope enlarged in terms of types of activities supported, and its name changed to '**Chips JU**'. This would build upon the strong knowledge base acquired by the ECSEL JU and its successor, the KDT JU. The KDT JU was one of the nine JUs set up by the so-called 'Single Basic Act'[28]. The change from the ECSEL JU under Horizon 2020 to the KDT JU under Horizon Europe led to an adaptation to the changing geopolitical situation and continued technological convergence. The scope was extended, going beyond microelectronics to relevant aspects of photonics, beyond embedded software to relevant higher layers of software, beyond Smart Systems to enable intelligent Systems of Systems (SoS), and addressing important trends including the emergence of new computing paradigms, edge-computing and its link with cloud computing – in particular for AI applications[29].

The Chips JU would have the responsibility for the implementation of four components of the Chips for Europe Initiative, namely:

- design capacities for integrated semiconductor technologies;
- pilot lines for preparing innovative production, and testing and experimentation facilities;
- advanced technology and engineering capacities for quantum chips; and
- a network of competence centres and skills development.

The fifth component of the Chips for Europe Initiative, the 'Chips Fund', would not be implemented by the Chips JU.

The amendment of the Single Basic Act (SBA), would add capacity building activities to the research and innovation activities currently supported by the KDT JU. Whereas the SBA set up the KDT JU, defined its objectives, bodies, and governance, and laid down the provisions to ensure a smooth transition from its predecessor, the SBA amendment makes relatively minor changes to prepare the KDT JU for the implementation of the Chips for Europe Initiative, to adjust its governance accordingly, and to introduce capacity building activities. Such activities would strengthen and promote Europe's capacities in semiconductor areas through large-scale deployment. Capacitiy

[28] Council Regulation (EU) 2021/2085 of 19 November 2021 establishing the Joint Undertakings under Horizon Europe and repealing Regulations (EC) No 219/2007, (EU) No 557/2014, (EU) No 558/2014, (EU) No 559/2014, (EU) No 560/2014, (EU) No 561/2014 and (EU) No 642/2014.

[29] See draft partnership proposal for the Key Digital Technologies Joint Undertaking, in particular section 2.2.5. https://ec.europa.eu/info/files/european-partnership-key-digital-technologies-kdt_en

building activities under the Chips JU would be funded via the Digital Europe Programme and would be limited to the four components of the Chips for Europe Initiative; they would not cover the full scope of the current KDT JU.

In addition, the Chips Act and the SBA amendment would increase the support for the JU's research and innovation activities, funded via Horizon Europe. It should be noted that many activities that would be considered research and innovation activities on the four components of the Chips for Europe Initiative are currently supported by the KDT JU and previously by the ECSEL JU. Examples are research and innovation activities on pilot lines supported by ECSEL (see Annex 5 for detailed examples) and the development of open-source RISC-V building blocks under KDT Work Programme 2021[30].

Apart from the introduction of capacity building activities for the four components of the Chips for Europe Initiative, coverage of the Chips JU would not be substantially different from that of the KDT JU. Decisions on adjusting scope in work programmes of the Chips JU would follow the governance rules as outlined in the SBA amendment (see also Chapter 9).

Given the importance of the semiconductor sector for downstream industries (see e.g. Section 2.4), it is expected that the Chips JU will take advantage of synergies with other European Partnerships. The Chips JU, for example, would be well positioned to cooperate with partnerships in mobility, e.g. on the development of chips and control systems for autonomous vehicles[31]. Similarly, cooperation could be established with partnerships in energy, health, agriculture, and other industrial sectors. In addition, cooperation with other digital partnerships is expected.

The Chips JU was proposed to have a total Union contribution of EUR 4.175 billion and a commensurate contribution by Participating States. Further explanation and details are provided in Chapter 10 and the legislative and financial statement (LFS) accompanying the proposed Chips Act.

8.1.9 The role of the European Chips Infrastructure Consortium (ECIC)

The Chips Act introduces the possibility to establish one or more European Chips Infrastructure Consortia (ECIC) – a mechanism to facilitate the implementation of different parts of the Chips for Europe Initiative, including for example the set-up of the new pilot lines. The main aim of an ECIC is to encourage effective and structural collaboration between legal entities, including Research and Technology Organizations and Member States. To enhance collaboration, the ECIC has to involve the participation of at least three legal entities from three Member States (these legal entities could be Member States themselves).

The use of the ECIC instrument offers several advantages over existing instruments in terms of autonomy, flexibility, and duration. An ECIC would have legal personality, and sufficient autonomy to lay down its membership, governance, funding, budget, the modalities by which the respective financial contributions from the members are called upon, and coordination, management and working methods. The members of the consortium would have full flexibility in determining applicable law, statutory seat, voting rights or any other incorporation or operational legal provisions

[30] The resulting IP libraries could be part of design capacities for integrated semiconductor technologies. For the KDT Work Programme 2021, see https://www.kdt-ju.europa.eu/wp2021.

[31] The connected, cooperative & automated mobility (CCAM) partnership would be an appropriate partnership for such cooperation.

as long as the proposed set-up would not contradict the conditions of the Chips for Europe Initiative and the objectives of the Chips Act. The process to set up an ECIC is set out in Article 7 of the Chips Act: the coordinator would submit an application to the Commission; the Commission would review the application based on the conditions provided in the Chips Act and if all conditions are met, adopt an implementing act setting up the ECIC. The Commission would not be part of the ECIC Consortium.

The ECIC would implement one or more activities foreseen by the Chips for Europe Initiative, for example the new pilot lines. For this, the Chips JU would launch a call for expression of interest, calling for an ECIC to implement the specific activity. The ECIC would receive budget from the EU and interested Member States to be shared and implemented on the basis of the particular ECIC setup and in line with State aid rules; the exact procedure for doing so would be established by the ECIC itself.

The procedure and the details for the expression of interest of an activity to be implemented by an ECIC are not provided in the proposed Chips Act nor in the amendment to Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (Single Basic Act, 'SBA'). This would have to be decided in the Work Programme of the Chips JU as an implementing body of the Initiative.

In this call for expression of interest, the ECIC would be asked to apply in order to implement the specific activity under the Initiative, by providing among others the following: a technological roadmap, the financial construct of the activity, including the Union contribution, the implementing partners, the implementation timeframe, the general rules for the IP policy on which the ROI could be carried out. If the ECIC is selected, it will become the implementing entity of the specific activity of the JU's work programme.

The mechanism provided by ECIC has a number of advantages over other instruments such as a JU. Firstly, it allows to **combine funding** from Member States, the Union and from the private sector, including throughout **a longer timeframe than the current Multiannual Financial Framework (MFF)**. Secondly, having legal personality, an ECIC could also engage in the **contracting of loans** (for example, through the EIB), to be repaid through revenue-generating activities such as IP creation and pilot lines' services. Thirdly, the ECIC could **own the infrastructure** and develop and **manage its intellectual property.** This could attract new business players; e.g. pilot lines may develop IP that would be essential for future production facilities or support the preparation of production nodes below 2 nm, strengthening collaboration with the First-Of-A-Kind production facilities foreseen in Pillar II of the Chips Act. Additional Member States and private partners could join the ECIC and financially contribute to its activities over time; Member States' contributions to the ECIC will be counted as national contributions to the JU. **A single ECIC would give further advantages**: maximise the synergies between the constituent pilot lines and the resulting benefits outlined above as in more power in purchasing tools and module development; reducing redundancies in operations; sharing experiences, libraries and IP; offering a single point of contact and legal entity in operating the lines; and creating a single, shared resource with critical mass by pooling the resources of all participants.

The ECIC implementation roadmap can adopt a phased approach to project development i.e. the first phase focusing on research aspects, equipment and other developments necessary for establishing the new pilot lines, followed by the second phase of their operationalisation and service provision. This phased approach would guarantee that the required budgets would be made available by the Member States and any private sector participants during the projected period of the pilot line operation, thus respecting the timeframes for implementing these pilot lines.

8.1.10 The Chips Fund

To develop a thriving semiconductor ecosystem, easier access to finance and investment opportunities for SMEs are needed. Overall, start-ups and scale-ups represent an important source of innovation, and their growth is essential to fuel a dynamic and forward-looking ecosystem. In Europe, innovative deep-tech semiconductor SMEs (including the ones addressing quantum technologies) face financing challenges over a long period, before returns are generated. Fabless companies incur into substantial costs for development, licensing IP and tools, prototyping and contract manufacturing, before they can generate any revenues, and without adequate financial support, they are often vulnerable to foreign acquisitions or brain-drain.

Financing these semiconductor companies requires an understanding of the characteristics of the industry and the needs for significant investments with a longer-term horizon. To address this need, a dedicated semiconductor investment facility was proposed to be established in the Chips Act package: **the Chips Fund**. This would provide increased availability of loans, venture capital financing and specialised funds, including equity investment solutions created through targeted investment facilities with the participation of the European Investment Bank (EIB) group, other financial institutions and private equity partners.

Firstly, for high-potential start-ups needing support to validate their technology and transform it into innovation, the **EIC** (European Innovation Council) **Accelerator** programme of Horizon Europe will offer a thematic challenge in the area of semiconductor technologies and quantum chips. This instrument will deploy up to EUR 300 million, potentially generating a multiplying effect of a factor 3 in private investments, addressing early investment gaps in the form of grants and equity, to help start-ups generate novel IP and mature their technology, thereby attracting further investors.

Secondly, for SMEs requiring financial support to scale-up their efforts and bring innovation to market, the **InvestEU Fund**, will offer dedicated financial products to be implemented by the EIB Group, International Financial Institutions and national promotional banks (NPBs) through financial intermediaries, such as venture capital or private equity funds. A dedicated budget to support investments in semiconductor chips and technologies will secure a guarantee of up to EUR 250 million, , for funding companies playing a role in the semiconductors value chain, from technology development to design and system integration, which is expected to leverage about EUR 1.2 billion of equity-based financing with other market investors.

Further, in the InvestEU Guarantee agreement with EIB Group, semiconductors are identified as an area of priority for investment. The EIB is ready to provide substantial resources in the form of loans and venture debt to support projects in line with EU ambitions, such as in the area of manufacturing, pilot lines, and technology infrastructures.

8.1.11 Impact and benefits

Establishing a technology infrastructure based on a model of openness and inclusiveness as described above will **accelerate the flow of innovation** and **strengthen the microelectronics ecosystem** in Europe. It will provide the stakeholders (see below) with **easier and faster access** to the design and piloting infrastructure. The work will be organized in the form of a series of intimately connected projects with specific focus, well-defined interactions and with a clear business case in mind.

The technology infrastructure, through the involvement of competence centres and the EDIHs, will act as an **aggregator of customer requests** (in particular from SMEs and start-ups) and bundle them into runs in pilot lines or commercial fabs. The direct benefits will be (i) **substantially lower costs**

of accessing the technologies being piloted; and (ii) an **acceleration of the innovation cycle** with seamless design, prototyping and manufacturing processes resulting in faster development of products.

Emerging design solutions, such as ultra-low-power energy-efficient processors, or processors and accelerators for different vertical sectors based on the open-source RISC-V computing architecture, will be tailored for feeding into sectors including automotive, energy, and medtech. The R&I activities would lead to IP blocks that could be part of libraries that would become an essential component of the design platform.

For the pilot lines, research and innovation activities would develop – for example – technologies to achieve transistor sizes below 2 nm, novel materials, as well as heterogeneous and 3D integration of different materials. Such R&I activities could be performed together with ongoing research on advanced materials, thereby contributing to HE Cluster 4 objectives.

Finally, by validating new processes before transfer to IDMs, the new pilot lines will enable participating companies to **commit to invest in the next generation of chips**, as outlined in articles 10 and 11 of the Chips Act.

In summary, the **specific benefits for European stakeholders** expected from Pillar 1 are:

- ***SMEs and start-ups*** will have **easier and faster access to foundry services** via a single point of contact, and lower development costs due to support in design and system integration and the use of cost-efficient options such as multi-project wafer (MPW) runs.

- ***Industry users and product developers*** will have **easier use of design tools and libraries** as well as **early access to advanced technologies**, through pilot lines for testing and experimentation and through foundries for volume manufacturing and heterogeneous integration. They will be enabled to **design innovative components and new system concepts** and **demonstrate key functionalities** such as new approaches to high performance, low energy, security, new 3D and heterogeneous system architectures, etc.

- ***Researchers*** will have access to and the use of **advanced facilities for developing, testing and refining** new technology concepts and prototypes.

- ***Equipment manufacturers*** will **develop, validate and demonstrate** their latest models in an advanced pre-production environment.

- ***Design companies*** will have **access to design libraries** and, through the pilot lines, be able **to develop and refine their EDA tools and IP** for advanced technologies and at leading edge nodes, thereby increasing their own product portfolio and businesses.

- The ***European ecosystem at large*** will be more easily **address their needs and requirements** and have wider, democratized **access to highly developed and expensive technologies** for key sectors such as automotive, industrial automation, communications, and healthcare, and **improved support by lowering the barrier to prototypes** and enabling small volume production, as well as opportunities and facilities for skills development and **developing a trained workforce** (see 8.1.4 above).

8.2 Pillar 2. A Framework to Ensure Security of Supply

8.2.1 Urgency to invest in new production capabilities for the EU

The supply chain disruptions and the shortages addressed in chapter 2 are symptoms of **the EU's excess dependency on production capacities located in third countries.** The EU's share of the global production capacity has been declining over the past 20 years. Moreover, the EU currently has no foundries that offer advanced manufacturing of components with feature sizes below 22 nm while the majority of capacity in the EU is still concentrated at 28 nm and above. The EU thus relies on imports for chips (for both leading-edge and mature nodes) that are then embedded in products manufactured by its industries, including automotive. In 2021, the EU exported semiconductors for a value of EUR 31.5 billion and imported for EUR 51 billion, i.e. with a deficit of EUR 19.5 billion (section 3.2).

Sections 3.2 and 3.3 illustrate the limited investments in the EU in the semiconductor sector (with about 4% of global capital expenditures since 2010 – see figure below). This led to a situation where the EU now only has a share of manufacturing capacities (7.2% of global market share in 2020) which is not commensurate with its economic weight and the needs of its industries. This exposes the EU to excessive dependencies.

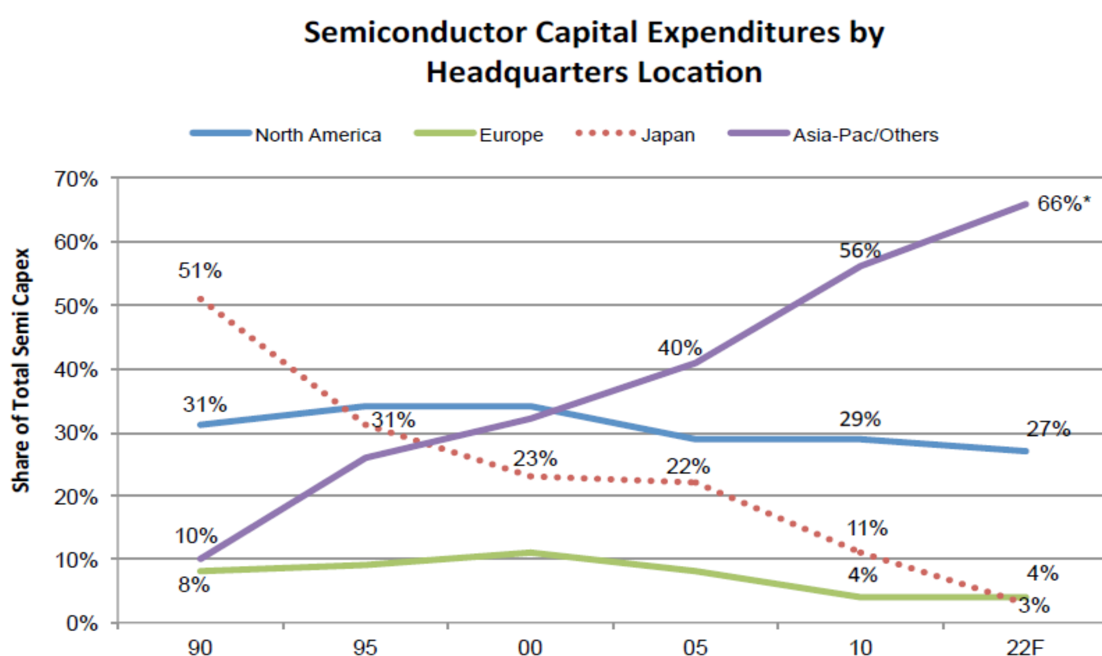

Figure 43. Evolution of capital expenditure in semiconductor sector by region (based on headquarters location – Source IC insights 2022)

Limited investment in production capacity is a consequence of the high costs and complexity of production of chips, which increase as chips become more advanced, and of an uncertain business model (see section 1.2.1). A leading-edge fab typically requires an investment of several billion euros. Taiwan and South Korea currently are the only countries in the world with leading-edge manufacturing capacities covering node sizes smaller than 5 nm and below. The fabs now active in the EU only produce advanced and mature nodes, whereas the application of cutting-edge chips in the

future is expected to increase across many application areas. This will notably concern critical sectors (such as health, transport or energy) and sectors which can still be considered as European strongholds (such as automotive) (see Chapter 4).

As semiconductors have clearly become a **strategic technological area**, the EU needs to **reinforce its capacity in the production of mature nodes** (10 to 28 nm), essential for the functioning of its economy, while at the same time **preparing for investing in production of nodes smaller than 10 nm**, which offer significant growth potential. Technological advances also need to be fostered on other important aspects than miniaturization, such as the use of innovative materials or processes or, for example, the improvement of chips manufacturing circularity (water consumption and reuse, and energy-efficiency) (see Chapter 5).

Furthermore, in view of the time needed to develop, build and setup manufacturing capacities, **it is of the utmost importance to invest now.** Today's efforts will shape the type and scale of production capacity available in the EU in 2030. A semiconductor fabrication plant typically requires two years to build and another one to two years to optimise production processes. Investments now will allow increasing production capacity in the EU as of 2025-26 in more mature nodes. And investments now in leading-edge nodes, starting with advanced pilot lines, are needed to develop knowledge and skills and be able to translate such investments in new production capabilities at 2 nm or below around 2028-2030 in Europe.

Without rapid and sufficient investments, Europe's market share could drop to less than 5%, given the doubling of the market and the scale of efforts taking place now in other parts of the world. **In the very recent years, the governments of China, the United States, Japan and South Korea took measures to support through incentives their local industrial ecosystems.** These countries support their chips industry with direct subsidies, tax exemptions, preferential customs and tariffs treatment, tax incentives to support innovation, investment funds, and regulatory action[32]. As part of the 'Made in China 2025' plan[33], the Chinese government allocated USD 150 billion over ten years to the sector with the ambition to reach 70% of self-sufficiency by 2025. The US Chips Act[34] should provide USD 52 billion of subsidies to support investments in R&D and semiconductor manufacturing in the United States until 2026. South Korea plans to support its semiconductor industry through tax incentives for its domestic companies' private investments in R&D and manufacturing, which are estimated to total USD 450 billion until 2030[35].

In view of the very high and still increasing capital intensity of the semiconductor manufacturing sector[36], private investment may likely require public **support with a view to achieving EU's ambition to reach 20% of global market share by value in leading edge semiconductors**[37] and **ensuring access to green, secure and trusted chips in Europe.**

With a framework for facilitating the establishment of **first-of-a-kind facilities**, the actions proposed under the second pillar of the Chips Act aim at contributing to **the EU's security of supply and strengthening of a resilient semiconductor ecosystem.** The expected resulting effect on production

[32] https://www.institutmntaigne.g/essuces/dfs/ublicatins/eue-new-gelitics-technlgy-1.df
[33] https://csets.cngess.gv/duct/df/R/R46767
[34] https://www.cngess.gv/bill/117th-cngess/senate-bill/1260?s=1&=52
[35] https://sectum.ieee.g/suth-keas-450billin-investment-latest-in-chi-making-ush
[36] The CAPEX as a percentage of the semiconductor market has significantly increased between 2010 and 2021, from 13.83% to 25.37%.
[37] See COM(2021)118 – 2030 Digital Compass: the European way to the Digital Decade.

capacities in Europe should also help ensure the security of supply of leading-edge components in particular while these are likely to become essential to many sectors (see Chapter 4).

The EU aims to be able to master and develop technologies that are pervasive to its digital economy. Advances concern performance but also energy-efficiency, security and data protection: the **development of more sustainable, trusted and secure chips** is an important objective of the pillar.

Leading-edge manufacturing capacities, including related foundry activities, are expected to have a positive impact on the pan-European ecosystem, stimulating the further development of fabless (or fab-lite) companies, advanced equipment and material suppliers, as well as fuelling the activities of RTOs. This should also be conducive to creating, retaining and attracting talents throughout the EU.

8.2.2 Explaining further the pillar 2 approach

The Chips Act proposes a framework to facilitate the implementation of projects that contribute to the security of supply and strengthen the resilience of the semiconductor ecosystem in the EU. Private investment in these facilities will likely require significant public support. Focusing public support on innovation is essential to ensure the longevity of public investment and limit the distorting effect on competition. Innovation could be recognised in different dimensions, ranging from process to product to energy performance. The Chips Act defines the concept of "first-of-a-kind facility in the Union" to provide guidance how such innovation should be demonstrated for the purpose of the Chips Act, i.e. in order to be recognised as an "Integrated Production Facility" or "Open EU Foundry". The Commission has already announced in the Communication "*A Chips Act for Europe"*[38] that it will also take this element into account for a possible State aid approval based on Article 107(3)(c) TFEU.

Under Article 107(3)(c) TFEU, the Commission may consider aid to facilitate the development of certain economic activities or of certain economic areas to be compatible with State aid rules, where it does not adversely affect trading conditions to an extent contrary to the common interest. To assess whether the aid does not adversely affect trading conditions, the Commission weighs the positive effects of such State aid against its likely negative impact on trade and competition for each individual case. Such positive effects include "pan-European" factors, such as a positive impact on the semiconductor value chain with regard to ensuring the security of supply and increasing qualified workforce, or its positive impact on the innovation potential of SMEs and verticals that can access innovative products at their doorsteps, or any other benefit that can be shared widely and without discrimination across the EU economy. As part of this overall balancing, the Commission will take into account that a new production facility is "first-of-a-kind" in the Union.

Under the proposed framework of the Chips Act, semiconductor manufacturing facilities would be able to receive a label that determines that these are "first-of-a-kind" facilities in the Union. The framework includes provisions to facilitate the establishment and operation, while requiring that these projects comply with criteria to ensure they contribute to the objectives and that they remain a reliable supplier of chips in a crisis. The two separate procedures for the recognition and for authorisation of State aid, where applicable, will be conducted in parallel (see the section 'Procedures' below).

[38] COM(2022) 45 final. See also the Questions and Answers available at https://ec.europa.eu/commission/presscorner/detail/en/QANDA_22_730

First-of-a-kind facility in the Union. In order to address the market failures as laid out above (see section 8.2.1), the Commission announced that it may authorise public support for the establishment of "first-of-a-kind" facilities in the Union.

This approach will be fully complementary to existing frameworks based on Article 107 TFEU and does not limit further possibilities to grant State aid, where these would also apply to the project in question. It is in particular complementary to the framework of Important Projects of Common European Interest (IPCEI) based on Article 107(3)(b) TFEU, which is intended to support multi-country R&I projects up to first industrial deployment in areas of common interest, thus supporting a different stage of the innovation cycle.

The Chips Act provides for a definition of such a "first-of-a-kind" facility. According to Article 2 (10), this would be defined as "an industrial facility capable of semiconductor manufacturing, including front-end or back-end, or both, that is not substantively already present or committed to be built within the Union, for instance with regard to the technology node, substrate material, such as silicon carbide and gallium nitride, and other product innovation that can offer better performance, process innovation or energy and environmental performance".

In essence, to be recognised as first-of-a-kind, a facility would need to offer a dimension of innovation that is not yet present in the EU. This innovation could be, for example, with respect to process, product or performance. This applies to projects for any production node, whether leading-edge or not. The definition provides an indicative list of these qualifying factors, e.g. the use of novel substrate materials such as silicon carbide and gallium nitride, smaller nodes, new functionalities or environmental performance of the chip. Innovation can be recognised in different dimensions. A suitable reference to identify the areas where such innovation can take place is the IEEE International Roadmap for Devices and Systems (IRDS), which identifies key technological trends related to devices, systems and all related technologies.[39]

A manufacturing facility of a comparable innovation capability should not yet be **substantively present** or committed to be built in the EU. This means that a manufacturing facility capable of producing a comparable product, process or performance at an industrial scale should not yet exist or currently be under establishment in the EU. In turn, if such innovation was already in use in R&D or small-scale production in the EU, this would not necessarily exclude new mass production qualifying as "first-of-a-kind". For instance, a manufacturing facility planning to use a novel substrate material could qualify as "first-of-a-kind" in the EU, despite this substrate material being tested in a pilot line in a Member State.

In this respect, it should be noted that it is not excluded that several parallel projects may be recognised as first-of-a-kind if each of them does not crowd out existing or planned private activities and if there is no risk of overcapacity.[40]

Framework for a label for "first-of-a-kind" facilities. To encourage investments in new production capacity, while at the same time ensuring these are to the benefit of the EU as a whole, the Chips Act

[39] This builds on the previous work of the ITRS, which also defined the reference for the process nodes (in nanometres) resulting from the evolutions of transistor scaling, in line with the prediction of Moore's law. The IRDS currently includes work by different International Focus Teams on the following fields: More Moore (scaling); More than Moore; Beyond CMOS; Systems and Architectures; Packaging Integration; Outside System Connectivity; Cryogenic Electronics and Quantum Information Processing; Lithography; Yield enhancement; Metrology; Factory Integration; Environment, Safety, Health, and Sustainability.

[40] See footnote 56 of the Communication, A Chips Act for Europe, COM(2022) 45.

proposes a framework for the implementation of two types of "first-of-a-kind" facilities. These two types reflect the two common business models of semiconductor manufacturing facilities in today's semiconductor industry landscape.[41] **Integrated Production Facilities (IPF)** are vertically integrated semiconductor manufacturing facilities, which are involved in front-end manufacturing[42] as well as in the design of integrated circuits or the provision of back-end services[43], or both. **Open EU Foundries (OEF)** are semiconductor manufacturing facilities which dedicate at least a certain extent of their production capacity to produce chips according to the design of other companies, in particular fabless companies. The framework proposes that companies could apply to the Commission to receive the label of Integrated Production Facility or Open EU Foundry for their planned facility.

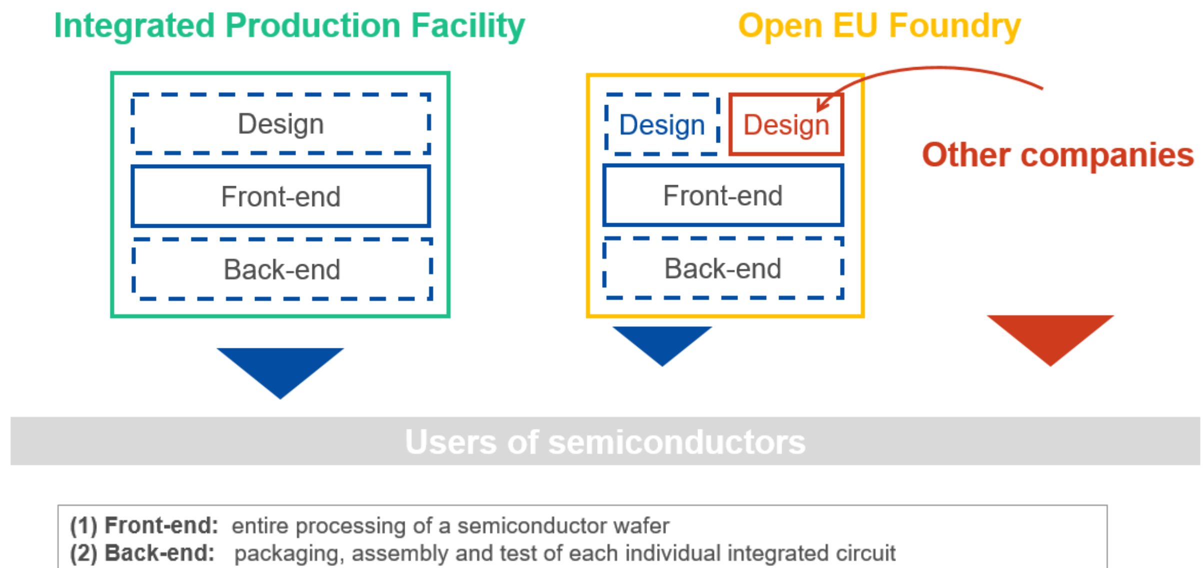

Figure 44. Comparison of the business models for Integrated Production Facilities and Open EU Foundries.

Criteria to ensure security of supply. To achieve the objective of increasing security of supply and strengthening the resilience of the EU's semiconductor ecosystem, these facilities would have to comply with certain criteria in order to qualify for the label. The purpose of these criteria is to ensure that these facilities contribute to the objectives, as well as to ensure they remain a reliable supplier in a shortage crisis.

- First, their establishment and operation would need to have a **clear positive impact on the Union's semiconductor value chain** with regard to contributing to the security of supply and increasing qualified workforce. The impact on the EU's value chain would be considered on a case-by-case basis.
- Second, they would have **to guarantee not to be subject to the extraterritorial application of public service obligations of third countries** in a way that may undermine the

[41] For an overview of the prevailing business models in the semiconductor industry, please refer to Section 1.2 (Global Semiconductor Value Chain).
[42] 'Front-end' means the entire processing of a semiconductor wafer (Article 2 paragraph 12). The front-end manufacturing activities by Integrated Production Facilities or Open EU Foundries could cover one or all steps in the processing of a semiconductor wafer, starting from various substrate materials (Si, SiC, SOI…).
[43] 'Back-end' means the packaging, assembly and test of each individual integrated circuit (Article 2 paragraph 13).

undertaking's ability to comply with their obligations under the Chips Act[44]. Hence, if Integrated Production Facilities or Open EU Foundries could expect to be subject to a public service obligation from a third country as well as a conflicting obligation from the Commission, they would be requested to organise their production capacity and sequence in a way to ensure the obligations imposed by the Commission can be fulfilled. Such guarantee could for instance be given via written statement and would need to include the commitment to inform the Commission if such instance arises.

- Third, they would need to provide a **clear commitment to invest in the next generation of chips**. Such a commitment could entail, for example, the commitment to contribute to the implementation of pillar 1 through providing knowledge and skills in preparing pilot lines, closely following and contributing to the development of those. Equally, the content of such a commitment could be having a pre-production facility installed in their facilities, for taking the results of the pilot line effort from the lab (e.g. the RTO) to the fab. The commitment could be demonstrated through preparing to invest in more advanced technological nodes (improving computing power and energy efficiency) or contributing to the preparation of pilot lines, or having pre-production facilities on their premises etc.

Benefits of receiving the label. Companies or consortia of companies could apply to the Commission to recognise their initiative as Integrated Production Facility or Open EU Foundry. This would lead to receiving the label as either type of facility. This is a separate procedure to the State aid assessment and, where applicable, these two procedures would be conducted in parallel. Receiving the label would entail several benefits:

- First, the Chips Act provides for **a streamlined approach to administrative applications**. These provisions are designed to address typical barriers to the implementation of large scale semiconductor manufacturing facilities, pertaining to the extensive time required for projects to acquire administrative permits and complex and fragmented permit-granting processes.

  Under Article 14, projects with the label would benefit from fast-tracking of administrative applications, such as environmental assessments and spatial planning. Where possible under national administrative law, they would be allocated a priority status. Furthermore, the Chips Act provides that the security of supply of semiconductors may be considered an imperative reason of overriding public interest within the meaning of Article 6(4) and Article 16(1)(c) of Directive 92/43/EEC (the "Habitats Directive") and Article 4(7) of Directive 2000/60/EC (the "Water Framework Directive"). The aforementioned directives allow in exceptional circumstances that projects may be implemented despite receiving a negative environmental assessment, if certain conditions are fulfilled and there is an imperative reason of overriding public interest[45]. The proposed provision in the Chips Act would clarify that the planning,

[44] Integrated Production Facilities and Open EU Foundries could be obliged to accept and prioritise certain orders for critical sectors in line with Article 21 paragraph 1 of the proposal (see section 8.3.3).

[45] For instance, Article 6(3) of the Habitats Directive requires appropriate assessment ("AA") of plans and projects that are likely to impact a Natura 2000 site. By way of derogation from the provisions of Article 6(3), a planned facility could be authorised for which the AA concludes a negative assessment of the implications for the site in view of its conservation objectives. In this case, the deciding authority would have to establish that all conditions of paragraph 4 of this Article, which is providing for the possibility to derogate, are met. This requires that no alternative solutions are available and that the facility is necessary for 'imperative reasons of overriding public interest'. It would also be necessary to demonstrate that compensation measures, which ensure that the overall coherence of the Natura 2000 network is maintained, have been secured. Article 14 paragraph 3 of the Chips Act proposes that the security of supply of semiconductors could be such an 'imperative reason of overriding public interest'. Since Integrated Production Facilities and Open EU Foundries would be considered

construct and operation of Integrated Production Facilities and Open EU Foundries may be considered as being of overriding public interest in this context. This consideration is given in light of the importance semiconductor technologies, and more generally digital technologies, have as enablers for the sustainability transition.

Furthermore, the Chips Act requires Member States to implement a **'one-stop-shop' approach to permit applications** and enhance coordination of the administrative process (Article 14 paragraph 4). For this purpose, Member States should nominate an authority responsible for facilitating and coordinating all administrative applications related to planning, construction and operation of each Integrated Production Facility and Open EU Foundry. Such a nomination becomes necessary for each project after it has received the label. The approach to provide the above-described benefits of fast-tracking of administrative applications and a 'one-stop-shop' for administrative applications follows the example of another EU policy area: the Regulation on the guidelines for trans-European energy infrastructure[46] grants certain administrative benefits and foresees the possibility to derogate from EU environmental directives for key energy infrastructure projects. The list of these key energy infrastructure projects is updated by the Commission through a delegated act every two years. Most recently, such a proposal was adopted in November 2021.[47] The new list consists of 98 projects in the areas of electricity transmission and storage, smart grid deployment, gas, and cross-border carbon dioxide networks.

- Secondly, Integrated Production Facilities and Open EU Foundries would receive **priority access to the pilot lines set up under the Chips for Europe Initiative**, meaning, for example, that their application to use the pilot lines could be accelerated and preferentially treated, without excluding or preventing effective access by others.
- Thirdly, receiving the label would **determine that a facility is "first-of-a-kind" and contributes to the security of supply in the Union**. Separately, the Commission will also take this element among others into account in the possible State aid procedure based on Article 107(3)(c) TFEU, as announced in the Communication "*A Chips Act for Europe*".

Procedure. For the recognition of their (planned) project as Integrated Production Facility or Open EU Foundry, individual companies or a consortium of companies would be able to apply directly to the Commission. The assessment would consider compliance with the criteria for Integrated Production Facilities or Open EU Foundries and the viability of the project. For the latter, the proposal suggests that applicants submit the business plan evaluating the financial viability of the project, documentation of the experience of the applicant and a letter proving the readiness of the Member States(s) on whose territory the facility would be built to facilitate its set-up. This documentation would enable the Commission to target the label to projects with a demonstrated prospect of success. After an initial assessment of the submitted documentation, the Commission would consult the European Semiconductor Board, which is an advisory body established in the Chips Act and consisting of representatives from the Member States (see Chapter 9). If the Commission's assessment is positive, it would approve the recognition by a decision.

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to contribute to the security of supply of semiconductors, their planning, establishment and operation could provide grounds for such a derogation.

[46] Regulation (EU) No 347/2013 of the European Parliament and of the Council of 17 April 2013 on guidelines for trans-European energy infrastructure and repealing Decision No 1364/2006/EC and amending Regulations (EC) No 713/2009, (EC) No 714/2009 and (EC) No 715/2009 (OJ L 115, 25.4.2013, p. 39).

[47] COM(2021) 8409 final.

If a Member State would aim to grant State aid to the project in question, a notification by a Member State of the planned aid would ideally take place at least at the same time as the submission of the application for recognition under the Chips Act. The pre-notification phase could be used to ensure an alignment of both procedures for the State aid authorisation and the recognition of Integrated Production Facilities and Open EU Foundries. The respective assessments would be carried out in parallel, with coordination between the relevant Commission services regarding the compliance with the criteria for Integrated Production Facilities and Open EU Foundries respectively. The Commission services would aim to prepare simultaneous decisions, the timeframe of which would depend on the duration of the State aid assessment, depending on the merits of each individual case under review.

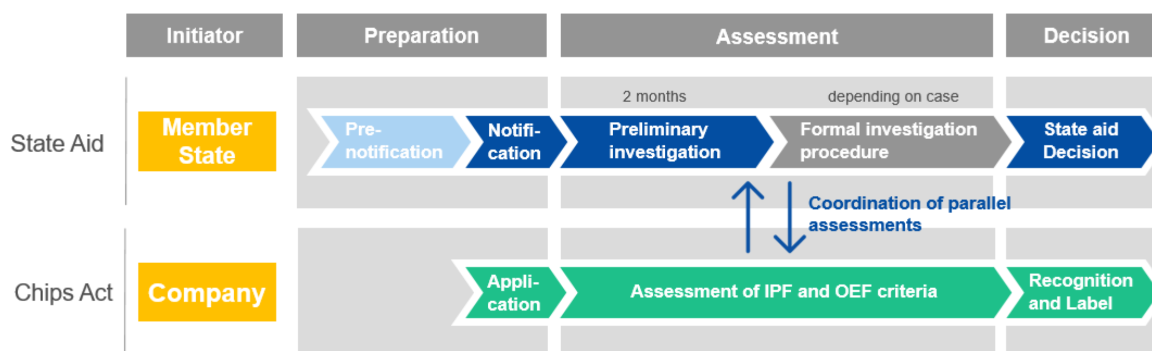


Figure 45. Comparative timelines of procedures of State aid notification and recognition as Integrated Production Facility or Open EU Foundry.

8.2.3 Impact and benefits

Maintaining a competitive semiconductor industry is crucial for the EU economy. Regions with a thriving semiconductor ecosystem derive several benefits such as industrial innovation, export opportunities, highly qualified and stimulating employment and overall economic growth. The examples below are to be read in the context of a need for supported projects to bring positive "pan-European" effects that can be shared widely and without discrimination across the EU economy.

In the global semiconductor industry, the average level of capital expenditures with respect to sales revenues has been consistently above 15%, even rising above 20% in the last few years (26% in 2021). If the average of 15% would be applied to the European industry, it would currently translate into a yearly capacity for capital spending of around EUR 6 billion, with the applicable future growth for the coming years. This gives a dimension of the level of investments that is reasonable to expect in the EU until the end of the decade.

The issue is that in the past 10-15 years, the level of CapEx investments of EU companies has remained stable, whereas that has steeply increased in other regions, with worldwide capital expenditures tripling in the last 10 years. The average investment share of EU companies has therefore gone down below 4% of global capital spending[48], as shown in figure 43.

Investments in production facilities in Europe in the past two decades was rather limited, as a consequence EU's share of worldwide capacity decreased from 11.7% in 2005 down **to 7.2%** in 2020 (see figure 19), with little presence in the more advanced digital nodes. The Chips Act could stimulate

[48] Source IC insights, McClean report 2022.

the potential for capital investment in the EU, contributing to building up the capacity necessary to respond to the growing demands of user industries.

Timely investments in manufacturing capacity are critical for the EU to successfully reach its ambitions. Initial investments in the 2024-25 period[49] would help to consolidate the position of the EU and a second wave of investments in 2026 to 2030 would drive an increasing market share towards the 20% objective by 2030.

The presence of semiconductor fabs in a region attracts the collaboration of many types of companies active in different fields across the entire value chain, such as design, testing, packaging, research and technology services, equipment and raw material, that generate additional innovation and economic value. The creation of Open EU Foundries should be instrumental in allowing to maintain and grow EU's semiconductor ecosystem overall, building on existing strengths outlined in section 3.3.

In order to master the complexity of such advanced technologies, close interactions among the different actors are required, therefore physical proximity is an important advantage. A well-known example is in the region that takes its name from the semiconductors industry that was born there, Silicon Valley, but that is not the only one. In Taiwan, for instance, in 1989 the government decided to promote the local development of the semiconductor industry and invested in a new Joint Venture with the Dutch chipmaker Philips, named Taiwan Semiconductor Manufacturing Company (TSMC), and that was the start of a flourishing local industry. Today in Taiwan, next to TSMC, which is a key player in the foundry market with over 56% share of global sales, there is UMC, the 3rd largest foundry, ASE, the global leader in back-end assembly, package and testing with 57% market share, Mediatek and Novatek, two of the world's largest fabless companies, as well as leading research and technology institutes such as ITRI and TSRI. This ecosystem, built around the first open foundry, makes Taiwan's industry the 2nd largest in the world, with an output of over EUR 100 billion per year, and an essential player in the global value chain.

In the EU, publicly funded fab projects have shown important positive effects as well. To take the most recent case, the new semiconductor fab of Bosch, which recently opened in Dresden (DE) following the fundamentally innovative know-how generated thanks to the support of the German government in the context of the first IPCEI on Microelectronics, has already demonstrated positive spill-over effects, connecting with the EU's semiconductor ecosystem (see box below).

[49] See for example the recent announcements of investments by Intel, as well as the collaboration between STMicroeletronics, GlobalFoundries, Soitec and CEA (https://www.cea.fr/english/Pages/News/roadmap-fdsoi-stm-soitec-gf-cea.aspx).

Example: BOSCH's new fab in Dresden, Germany

The IPCEI project laying out foundations for a new semiconductor site in Germany is still running, and so far it has produced the following spill-over results:

- Triggered private investments of approx. 1 billion EUR in microelectronics in the EU
  - Construction of facilities over 70,000 m^2 of floor space
  - AIoT facility in the EU: Fully connected and self-optimising, involving advanced automation technologies from several partners
  - Strong focus on demands from European users with leading-edge automotive technology capabilities
- Pushing the limits in know-how, skills and cutting-edge innovation
  - Creation of highly qualified jobs for up to 700 associates
  - Strong collaboration with European semiconductor ecosystem to foster skills in AI, Big-Data, technology development, process- and equipment engineering
- Cooperation with several European universities on education and training
  - More than 140 sensor training kits provided to students in 7 Member States; Mentoring of over 12 doctorate degree studies in several Member States
  - Development of sensor use cases for future mobility, smart agriculture, climate monitoring, resource efficient manufacturing logistics, smart health monitoring, and still many more to come
- Talent management and development
  - International student competition events for future mobility, IoT and sensor hackathon
  - Open Big Data Summer School with focus on MEMS sensors in Budapest
- Collaboration with new and existing partners in publicly funded projects
  - Partnering to continue IPCEI related technology development in several ECSEL/KDT projects
  - Partnering in several national and European R&I projects on trusted electronics
- MEMS Foundry Service
  - Bosch to open its technology capability to external partners
  - First projects started with two SMEs on LiDAR sensors and timing devices; one project with a large enterprise on MEMS substrate material
  - Active public offering via conferences, journals and internet
- Multi-design wafer runs
  - Set-up process to allow several MEMS designs to be integrated in one wafer run
  - Cost-efficient concept for universities and RTO's including student training; cooperation with universities in EU (e.g. Minho, PT)

Semiconductor fabs need to innovate continuously, and they are catalysts for further innovation across the entire technology ecosystem. They spur important investments in research and innovation. The semiconductor industry indeed is one of the most research-intensive sectors overall, spending 15-20% of revenues in R&D, and there is an important return on the investments. Public support for such R&D activities can well be justified. This is why specific State aid Guidelines exist for Research, Development and Innovation in Europe. According to a study from SIA, the US federal investments in semiconductor R&D have triggered an increase in the national gross domestic product that is 16 times higher[50].

[50] Study from the Semiconductors Industry Association https://www.semiconductors.org/wp-content/uploads/2020/06/SIA_Sparking-Innovation2020.pdf.

Investments in such ecosystems generate increased economic activities and incentivize **larger investments from the private sector in many downstream industries,** with a far greater financial impact, since semiconductor products are key enablers of applications in all sectors of the European economy and for the benefit of society. In addition to the direct impact of the activities of the semiconductor industry, we must consider the indirect impact of the upstream and downstream value chains. Beyond the turnover generated by chip manufacturers active in the EU, according to data from *DECISION*[51], in terms of value generated in the downstream electronics value chain, there is a multiplying factor of three times at the level of electronic assemblies, and eight times at the level of electronic systems.

Local semiconductor ecosystems can also generate **important employment opportunities, attracting and retaining talent and raising the skill levels.** According to Eurostat, in 2018 the EU 27 accounted for 219 000 employees in the manufacturing of electronic components, with an annual growth rate of 3% over the 2012-2018 period. *DECISION*[52] estimates that the microelectronics sector in the EU, including design and production of components, materials and equipment, is directly responsible for 455 000 high-skilled jobs. Moreover, as an enabling sector for the entire electronics value chain, from materials to systems, it accounts for 2.6 million jobs in total (see table 2). The demand for new skills is also increasing. The expected investments resulting from the establishment of the framework proposed under the second pillar of the Chips Act therefore could contribute to the creation of thousands of additional jobs in this and related sectors.

Sector	*Companies*	*Employees*
Materials & equipment	24	165 000
Electronic components	47	290 000
Electronic assembly	126	765 000
Electronic systems	290	1 350 000
TOTAL	487	2 570 000

Table 2. Employment in microelectronics sector Europe in 2018 (Source: DECISION[89])

In terms of induced employment, according to SIA and Oxford Economics[53], **for each worker employed by the semiconductor industry, an additional 5.7 jobs are supported in other sectors of the economy.** Therefore, the semiconductor industry has an employment multiplier of 6.7, one of the highest of any industry. In its recent announcement of investments in Europe, Intel specified that the new fab they plan to set up in Germany should employ around 3 000 highly qualified professionals, and that it would support 14 000 to 17 000 additional jobs in the broader economy, with an employment multiplier of 6.2.

[51] Study on the Electronics Ecosystem: Overview, Developments and Europe's Position in the World (EU 2018-19)
[52] Analysis of skills needs and occupational profiles for microelectronics (METIS programme 2020-21)
[53] Study from Oxford Economics and Semiconductors Industry Association: https://www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf.

Furthermore, advances in production processes often include **improvements on energy-efficiency and environmental impact of factories** and are consistent with the European Climate Law[54]**.** Supporting the production of **more energy-efficient and environmentally friendly components throughout their whole life cycle** (i.e. production, operation, end-of-life) based on innovative approaches (e.g. the development of more efficient manufacturing technologies with a reduced use of energy and materials, the design of semiconductors able to operate with lower levels of energy) would also help limiting the growing impact of the sector on climate and environment. Thanks to technology advances, manufacturing fabs with advanced lithography equipment can produce chips at smaller nodes that are more energy efficient. Processor chips tend to reduce power consumption by nearly two-thirds every two years. Furthermore, power electronics chips, particularly the new generation based on Silicon Carbide, are the key enablers of electric mobility and of all power conversion and transmission systems of renewable energy sources. Therefore, the chips produced by these new facilities can greatly contribute to the achievement of the objectives of the EU Green Deal.

[54] Regulation (EU) 2021/1119 establishing the framework for achieving climate neutrality. 30/06/2021

8.3 Pillar 3. Monitoring and Crisis response

8.3.1 Urgency for the EU to start monitoring the semiconductor supply chain

Chips are ensuring essential functions in nearly every technology product today (see Chapter 1) and any shortage in their supply (such as the ones experienced over the past two years – see Chapter 2) can potentially affect many economic and social activities, including the most essential ones.

The supply of semiconductor devices is essential for some industries that are critical for the functioning of the EU's economy and society. This includes sectors such as energy, transport, finance, health, utilities, defence, and public safety and security. Among these critical sectors, several depend on specific types of chips that are difficult to substitute as they are designed in compliance with certain safety requirements (see, for example, section 2.4.2). Furthermore, critical sectors that typically purchase smaller quantities are struggling to buy semiconductors on the market in crisis situations in which foundries give preference to high volume demand (see, for example, section 2.4.3). This leaves critical sectors particularly vulnerable in shortages and hence, exposed to production disruptions. Other sectors of significant economic importance in the EU, such as automotive and industrial automation, also heavily depend on the supply of chips for their production.

An important lesson from the current shortage is that the **lack of availability of relevant detailed information** makes it difficult to establish a precise assessment of risks related to potential disruptions of supplies. There is a need for more data to be shared about production capacities, choke points, and needs of companies in critical sectors. Overall, similarly to what was already done in the United States[55], the EU needs to develop an in-depth understanding and increased transparency of global semiconductor supply chains. While the Commission is already working together with the Member States to understand fully the impact of the current supply disruptions on Europe's industrial ecosystems,[56] this emphasises the need for a permanent mechanism allowing continuous, effective and coordinated information gathering and exchange at EU level on a regular basis.

The current shortage has demonstrated the **need for improved tools to address emergency situations.** Firstly, there is no instrument at EU level to allow for ad hoc gathering of information that enables decision-makers to adapt their policy responses to the shift in conditions and shortages. Secondly, in view of the demonstrated vulnerability of critical sectors in a semiconductor shortage, there is a lack of solutions to ensure the appropriate allocation of products available to priority areas when necessary and avoiding complete disruptions for critical sectors.

In this context, **actions have been initiated at national level** in order to better anticipate and mitigate the effects of shortages[57]. Other Member States might decide as well to tackle the semiconductor shortages by means of national measures, in particular due to the significant impact of shortages on other (strategic) markets and economic sectors. Given the intrinsic cross-border nature of the

[55] The US Department of Commerce has conducted a survey and assessment of the state-of-play of its semiconductor industry. The results have been presented on 25 January 2022. (Source)

[56] In early 2022, the European Commission has carried out a targeted stakeholder survey ('EU Chips Survey') (https://ec.europa.eu/growth/news/stakeholder-survey-european-chip-demand-2022-02-16_en). The European Commission will publish an overview of the aggregated results of the EU Chips Survey as part of a Factual Summary Report during Q3 of 2022. These will help to provide crucial information on sources and impacts of the supply survey.

[57] Spain announced its intention to reform its National Security Law (*Ley de Seguridad Nacional*) and to cover, amongst other, semiconductors therewith. The envisaged law would allow to establish a list of critical products, monitor the production capacities, create a strategic reserve thereof, and introduce obligations for producers to ensure security of supply and possibly address priority needs in case of crisis situation.

concerned markets, the semiconductor crisis would be further aggravated with the adoption of new initiatives in some Member States, while other Member States that are equally impacted by the crisis might take no action. Without action at EU level, the resulting regulatory fragmentation would seriously undermine the functioning of the single market.

The Commission has therefore proposed in the Chips Act to **foster coordination at Union level to better anticipate and react to potential shortages of semiconductors.** Beyond the above-mentioned risk for the proper functioning of the single market, action at EU level would allow to address the issue in a more efficient way, notably in view of the structure of the semiconductors value chain, which features a high-level of concentration in some segments (see section 1.2.3).

Such cooperation between Member States and the European Commission will strengthen the EU's and Member States' abilities to react to crises related to disruptions of the semiconductor supply chain. It will also optimize the allocation of resources and increase the efficiency of relevant measures.

8.3.2 Explaining further the pillar 3 approach

The Chips Act proposes a mechanism for coordinated monitoring of the semiconductor value chain and crisis response to shortages of semiconductors. This would include a **monitoring scheme** under which the national competent authorities of Member States carry out regular observatory tasks and provide for a mechanism to receive updates on demand fluctuations from the industry. The information would be discussed in the European Semiconductor Board. Discussions would include an **early warning and crisis mechanism**, whereby Member States alert the Commission of potential shortages. The Commission would assess the situation and, if necessary, activate the semiconductor crisis stage via an implementing act. After such a crisis has been triggered, the Commission may use a set of exceptional crisis response measures from a **crisis toolbox**.

Monitoring: To address the current **lack of availability of relevant detailed information**, the Chips Act proposes a mechanism for monitoring of the semiconductor value chain. Member States should monitor certain **early warning indicators** for a potential shortage. The early warning indicators are to be developed by the Commission in the frame of a risk assessment of the semiconductor supply chain, based on information collected collaboratively with the Member States. The Chips Act gives an indicative list of what these indicators could be.[58] Lead-time for certain chip types is one of the most important indicators, but also price changes, for both output and input, abnormal fluctuations in demand, and logistics data. Knowledge of events disrupting the supply chain, such as military conflicts and natural disasters, will also play an important role. Furthermore, Member States should monitor the availability and integrity of the products and services of **key market actors**. Key market actors are important players in the semiconductor industry, essential to the functioning of the semiconductor supply chain in the EU. Business closures, delocalisations or acquisitions of these key market actors could have a disruptive effect to the semiconductor ecosystem in the EU. This should be taken into particular consideration, for instance with regard to foreign direct investment[59].

[58] Recital 37: Such indicators could include the availability of raw materials, intermediate products and human capital needed for manufacturing semiconductors, or appropriate manufacturing equipment, the forecasted demand for semiconductors on the Union and global markets, price surges exceeding normal price fluctuation, the effect of accidents, attacks, natural disasters or other serious events, the effect of trade policies, tariffs, export restrictions, trade barriers and other trade related measures, and the effect of business closures, delocalisations or acquisitions of key market actors.

[59] See for example: The Weak Links in China's Drive for Semiconductors, institute Montaigne, January 2021, (Table 6).

The proposed monitoring mechanism would include information exchange with user industries. The practical implementation could, for example, build on individual industry initiatives, which strive to anticipate the total effective demand for critical semiconductors such as microcontrollers and analogue chips. Such estimates can be a major challenge, as customers tend to overstate demands especially in times of shortages. Strong fluctuations in prices and inventory levels and long lead times are the regular consequence (bullwhip effect). It is in the interest of industry to moderate such fluctuations. Yet the industry initiatives are not sufficient as they look only at individual supply chains and do not cover all relevant end user industries. In the context of the Chips Act, the total effective demand per chip family could be recorded by aggregating company individual demands and then used to pre-empt shortages.

Pilots have been established in a series of publicly funded projects at EU and national level to create a trusted platform for demand forecast[60]. Such a platform allows chip producers and chip clients to declare chip-specific capacities and demands in an anonymised way and extracts with computational methods the actual demand. The data structures encompass entire semiconductor supply chains from the material suppliers up to the industrial end users of chips. As the platform uses semantic web methods, it is by construction scalable to very large user groups. This work has been in the research phase so far and, if implemented in the framework of the Chips Act, could be validated by industrial users and public authorities to capture early warning indicators for critical markets.

Early warning and crisis mechanism: To address the need for enhanced **coordination at European level to better react to potential shortages of semiconductors,** the Chips Act proposes a mechanism whereby the Commission would be obliged to convene an extraordinary Board meeting when it becomes aware of potential crisis – through an alert by Member State(s) or through other sources, including international partners. In addition, taking account of the global nature of the semiconductor value chain and the importance of international cooperation, the Commission would enter into consultation or cooperation with relevant third countries with a view to seeking cooperative solutions[61]. In the extraordinary Board meeting, the Board will assess together with the Commission whether it is warranted to activate the crisis stage. Furthermore, this extraordinary Board meeting would give rise to the opportunity for Member States to discuss with each other if it would be useful to start joint procurement of certain products, which would be carried out under the framework of Directive 2014/24/EU of the European Parliament and of the Council.[62]

The assessment to trigger a crisis would follow a two-step approach: First, there must be serious disruptions in the supply of semiconductors leading to significant shortages in the EU. Second, these shortages must either entail significant delays or negative effects on one or more important economic sectors, or prevent the supply, repair and maintenance of essential products used by critical sectors.

Emergency Toolbox: When the crisis stage is activated, the Commission would exceptionally be enabled to take certain emergency measures set out in the Regulation. The deployment of each measure would take place in dialogue with the European Semiconductor Board and would be limited to where necessary, appropriate and proportionate in accordance with the EU's international obligations. Out of the toolbox, several tools would be limited in use to the benefit of **critical sectors**.

[60] EU project, SAFE-DEED | Safe Deed; ECSEL project Productive 4.0 - A European co-funded innovation and lighthouse project on Digital Industry (productive40.eu); German research project Gaia-X: A Federated Secure Data Infrastructure

[61] International cooperation initiatives include EU-US Trade and Technology Council (TTC), and Digital Policy and Industrial Dialogues with South Korea, Japan, Singapore and Taiwan.

[62] Directive 2014/24/EU of the European Parliament and of the Council of 26 February 2014 on public procurement and repealing Directive 2004/18/EC (OJ L 94, 28.3.2014, p. 65).

The definition of critical sectors in the Chips Act builds on EU acquis by referring to the sectors listed in the annex to the Commission proposal for a Directive of the European Parliament and of the Council on the resilience of critical entities[63]. Additionally, the defence sector and other activities that are relevant for public safety and security are considered critical sectors for the purpose of the Chips Act. The Commission may further limit the scope of these measures to only some critical sectors.

The Emergency Toolbox will consist of several tools:

- **Information Requests.** To increase the understanding of the supply chain disruptions and enable decision-making in response to a crisis, the Chips Act proposes to empower the Commission to launch mandatory information requests about production capabilities and capacities, current primary disruptions and other existing data necessary to assess the nature of the crisis or to identify and assess potential mitigation or emergency measures to put in place. These would address representative organisations and, if necessary, individual companies operating along the semiconductor supply chain. These ad hoc information requests in a crisis would be complementary to the regular monitoring activities proposed in Article 15, in that the response to these requests would be obligatory and enforceable, with the objective to ensure rapid and efficient access to information necessary in the particular situation and be able to rapidly adapt policy decisions.

- **Priority Rated Orders.** To address the abovementioned lack of instruments to ensure allocation of resources in the EU in a shortage to particularly vulnerable critical sectors, the Chips Act proposes a priority rating obligation for certain companies operating along the semiconductor supply chain. The priority rating obligation entails the enforceable obligation to accept and prioritise an order of crisis-relevant products. This obligation would be enacted through a Commission decision addressed to the individual company, following a case-by-case assessment and only where necessary and proportionate, having regard for the legitimate aims of the undertaking and the cost and effort required for any change in production sequence. The Commission decision would specify the product, quantity and time limit. Any order would be placed at fair and reasonable prices. This obligation is limited in scope. Under Article 21, Integrated Production Facilities and Open EU Foundries, as well as semiconductor undertakings which have accepted such possibility in the context of receiving public support, could receive a priority rated order. This would be possible where necessary and proportionate to ensure the operation of all or certain critical sectors.

  Exceptionally, the scope may be extended to other companies operating along the semiconductor supply chain in the EU, if such a company is subject to a third-country priority rated order measures, and compliance with this obligation could significantly impact the operation of certain critical sectors. For this purpose, any company operating along the semiconductor supply chain in the EU would be obliged to inform the Commission when they are subject to a third-country priority rated order measure.

  The Chips Act provides safeguards for companies. Companies would have a right to redress; they may request the Commission to review the priority rated order, if they are unable to perform the order, or because fulfilling the order would pose an unreasonable burden and particular hardship. Companies which fulfil a priority rated order would in turn receive a liability protection for any breach of contractual obligations required to comply with such order (Article 21 paragraph 6).

[63] COM(2020) 829. 16.12.2020.

Similar tools are in use in other jurisdictions, including the USA: Priority rated orders are an instrument used for the purpose of national defence provided for under Section 4511, Title I (Prioritization and Allocation), of the US Defense Production Act. The Department of Defense (DoD) is the most frequent user of both Title I and Title III authority. It prioritizes about 300 000 orders each year under Title I for the purpose of national defence.[64] The DoD has primarily used Title III to mitigate critical shortfalls in domestic defence industries.[65] Notably, it has invoked Title III in December 2020 to sustain and strengthen industrial capabilities and defence-critical workforce in recovery of the pandemic.[66]

- **Common Purchasing**. As an additional instrument to ensure allocation of resources to priority areas, the Chips Act proposes a framework for common purchasing of crisis-relevant products. Against the background that certain critical sectors have experienced difficulties to purchase as foundries give priority to high volume demand (see, for example, section 2.4.3), common purchasing would allow to pool the negotiating leverage across the EU. Any use of this instrument would be on initiative of two or more Member States, with whom the responsibility for deployment or re-sale of the procured products would lie. The Commission would act as a central purchasing body and procure on behalf of the participating Member States. The participating Member States and the Commission would stipulate a framework agreement to lay down the specific conditions and procedure for the individual activation of this measure. The proposed centralised approach provides greater negotiating leverage, allowing the Commission to pool demand across the EU and offer greater procurement power for the benefit of critical sectors. [67]

- **Export Authorisations.** Export authorisations can be an effective instrument to increase the knowledge and transparency of supply chains. [68] Any such measure would be introduced under the Framework of Regulation (EU) 2015/479 on common rules for exports.[69] When the crisis stage is activated, the European Semiconductor Board would assess the expected impact of the possible imposition of such measures and provide a non-binding opinion to inform the Commission's assessment under the EU framework of common rules for export. The

[64] The Defense Production Act Committee Report to Congress 2019, (Source, p. 8).

[65] Usage of the Defense Production Act throughout history and to combat COVID-19 | Yale School of Management

[66] DOD Announces $74.9 Million in Defense Production Act Title III COVID-19 Actions (Press Release)

[67] Previously used similar tools: The Joint Procurement Agreement (JPA) enables the Commission to organise procurement of medical supplies on behalf of participating Member States. 12 procedures have been launched since 2020, allowing countries to order essential medical supplies for nearly €13 billion. The JPA is based on Art. 168(2) TFEU (support to Member States' cooperation in public health).
The Commission established a centralised approach to procuring COVID-19 vaccines on behalf of Member States, following an agreement between the Commission and Member States based on Council Regulation (EU) 2016/369 (ESI Regulation). The Commission also financed a part of the upfront costs from the €2.7 billion Emergency Support Instrument.

[68] Regulation (EU) 2015/479 of the European Parliament and of the Council on common rules for exports was used for an export authorisation scheme for COVID-19 vaccines, which was in place from 30 January until 31 December 2021. Introducing authorisations for exports of vaccines produced in the Union has helped to improve the transparency of vaccines production, deliveries and supply chains, and to secure deliveries to Europeans in line with companies' contractual obligations.

[69] Under this framework, the Commission is empowered to adopt an export authorisation scheme of six weeks through an implementing act in accordance with the examination procedure, or exceptionally the urgency procedure, in order to prevent or remedy a critical situation caused by the shortage of an essential product (Article 5). Furthermore, the Commission may for the same purpose adopt additional appropriate measures through an implementing act in accordance with the examination procedure (Article 6).

involvement of the European Semiconductor Board to provide a non-binding opinion allows the Commission to benefit from the expertise of the Board in this context.

Safeguards for security of supply: The Chips Act proposes additional safeguards for the security of supply. In the frame of receiving the label, Integrated Production Facilities and Open EU Foundries commit to inform the Commission about third-country public service obligations to which they are subject (Article 10(2)(c) and Article 11(2)(c)). Additionally, any company operating in the EU would have to inform the Commission about information requests from third countries related to their activities in the semiconductor sector (Article 20 paragraph 5). The rationale behind these safeguards is to inform the Commission of crisis measures arising from third countries. This allows early notification of a semiconductor shortage that may have arisen in a third country and not yet reached the EU. This information would additionally enable the EU to take measures to ensure security of supply if necessary and proportionate.

8.3.3 Impact and benefits

The impact of the current market disruptions (see section 2.4) has demonstrated the need to equip the EU with appropriate tools to anticipate and mitigate the effects of future shortages. The proposed mechanism for coordinated monitoring and crisis response addresses directly the shortcomings identified during the current shortage (see section 8.3.1), notably the lack of structured cooperation between decision-makers and lack of instruments for coordinated crisis response at EU level. It is expected that the proposed mechanism would enable regular coordination and information exchange, allowing to anticipate shortages and for a quicker and more efficient reaction to such, as well as an appropriate allocation of available products in case of severe shortages, with the objective to limit the consequences of shortages on critical sectors.

The proposed monitoring and crisis response mechanism follows a balanced approach *in that it introduces crisis response measures* ***only where these are necessary, appropriate and proportionate*** *in order to ensure supply to critical sectors and* ***in close dialogue with Member States and experts*** *through the European Semiconductor Board.*

The chosen approach does not foresee activities with marginal burden for national authorities and companies under regular operation, while effectively and efficiently enabling anticipation of shortages through an early warning system that foresees action only in the case of indicators of a potential disruption of supply of semiconductors. Any crisis response measure could be enacted only after activation of the crisis stage through an implementing act, allowing for full scrutiny by the Member States in the frame of comitology. For each crisis measure, appropriate safeguards ensure that any potentially burdensome action is taken only after careful evaluation whether this would be necessary, appropriate and proportionate, in close dialogue with Member States and experts through the European Semiconductor Board.

During regular operation of the monitoring and crisis response mechanism, expected activities from national authorities or business would relate to the collection and sharing of information necessary to put in place regular monitoring and early warning. National authorities may incur administrative burden with regard to retrieving necessary data for these monitoring activities and putting in place

solutions for secure exchange of such data with private entities, while it is expected that they could benefit from standardised solutions provided for in the European Semiconductor Board. Businesses responding to such requests would incur costs for the technical solutions to make the data available (see section 11).

The implementation of the proposed crisis measures may entail some direct and indirect impact on businesses and other private entities, which would be limited to exceptional situations and be carefully taken into account in each case to ensure they comply with the principle of proportionality. If enacted, the proposed mandatory information requests may incur costs for the technical solutions to make data available (see section 11). This impact would be proportional in light of the expected benefit as the information gathering would enable decision-makers to attain an in-depth understanding of the causes for disruption and to identify mitigating action. If enacted, the proposed priority rated orders are expected to directly incur cost for concerned businesses, in particular for the change in production sequence. Indirectly, customers of the concerned companies may incur costs due to delay or cancellation of their previously placed orders. To ensure this measure remains proportional, **the scope of priority rated orders would be focussed on companies that have likely benefitted from significant public support.** Furthermore, there is no equally effective tool to ensure that available resources are preferentially utilised for products supplied to critical sectors. Common purchasing may imply impact on competitors of the awarded contracting parties as well as on trade. To ensure that such a measure remains proportional, such activity would be subject to the application of the procurement rules of the Financial Regulation[70], which ensure transparent and open procedures. To focus this measure further, common purchasing would be deployed only to the benefit of critical sectors.

The proposed monitoring and crisis response mechanism is expected to reinforce the freedom to conduct a business provided for under Article 16 of the Charter of Fundamental Rights of the European Union (the 'Charter'), by strengthening the resilience to disruptions of the entire semiconductor ecosystem. Nevertheless, some crisis response measures may temporarily limit the freedom to conduct a business and the freedom of contract, provided for under Article 16 of the Charter, and the right to property, provided for under Article 17 of the Charter. Any limitation of these rights would, in accordance with Article 52(1) of the Charter, be provided for by the law, respect the essence of these rights and freedoms, and comply with the principle of proportionality.[71]

[70] Regulation (EU, Euratom) 2018/1046 of the European Parliament and of the Council of 18 July 2018 on the financial rules applicable to the general budget of the Union, amending Regulations (EU) No 1296/2013, (EU) No 1301/2013, (EU) No 1303/2013, (EU) No 1304/2013, (EU) No 1309/2013, (EU) No 1316/2013, (EU) No 223/2014, (EU) No 283/2014, and Decision No 541/2014/EU and repealing Regulation (EU, Euratom) No 966/2012.
[71] See for a detailed analysis of impact on fundamental rights: COM(2022) 46 final, p. 14, 15.

9. Coordination and Governance of the Chips Act

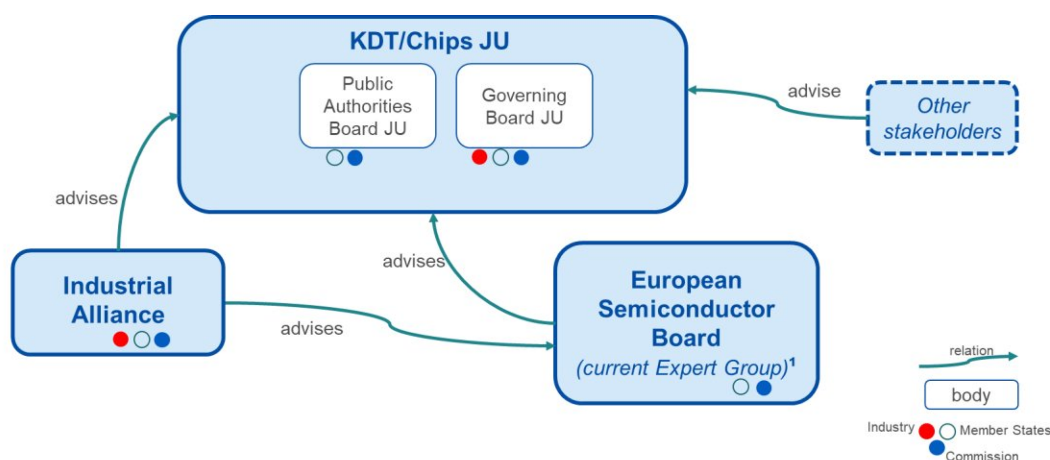


Figure 46. Overview of the proposed coordination and governance structure

The proposed **Chips Act** of 8 February 2022 includes the European Semiconductor Board as the overarching governance structure for the three pillars of activity. In parallel, the proposed amendment to the SBA ('SBA amendment') adapts the functioning of the renamed Chips Joint Undertaking to ensure a proper coordination between the Joint Undertaking (and its different bodies) and the European Semiconductor Board. At the same time, both the Chips Act and the SBA amendment include references to the Industrial Alliance on Processors and Semiconductor Technologies (the 'Alliance'): in the context of the Chips Act, the Commission may invite organisations representing the interests of the semiconductor industry to participate in the European Semiconductor Board in an advisory function or as observers, including, for example, members of the Alliance. In the context of the SBA amendment, it is proposed that the input from stakeholders, such as, but not limited to, the Alliance may be taken into account during the process for shaping the Joint Undertaking's work programmes.

The **European Semiconductor Board** set up by the proposed **Chips Act Regulation** would be a forum that facilitates cooperation and the exchange of information among Member States. Once the Chips Act enters into force, the Board would replace the **Semiconductor Expert Group** referred to in the **Recommendation** published on 8 February 2022. This Expert Group has already been set up to act as platform for coordination between Member States and to provide advice and assistance to the Commission. The Board would consist of representatives from the Member States and is chaired by the Commission. With regards to the Chips Joint Undertaking, the Board would provide advice to the Public Authorities Board (Pillar 1). The Board would also act as an advisory body with respect to Integrated Production Facilities and Open EU Foundries, as well as certification schemes (Pillar 2). Finally, the Board would serve as the coordination mechanism and be consulted in the frame of the monitoring and crisis response measures (Pillar 3). Additionally, it would support the Commission in the area of international cooperation and in the consistent application of the Chips Act.

The **Industrial Alliance on Processors and Semiconductor Technologies**[72] was set up by the Commission in 2021. It is not a body that would be established under the Chips Act or the SBA (amendment). The Chips Act proposes to include it as an advisory body into the governance system, along with other stakeholders. Similarly, the SBA amendment also makes references to roadmaps produced by the Alliance that may serve as advice or guidance to the Joint Undertaking's governing bodies. Dedicated working groups under the Alliance can address specific sectors, such as Defence and Space, to ensure proper representation and facilitate operations.

The SBA amendment would assign the responsibility for the execution of the **Chips for Europe Initiative to the Chips JU** – with the exception of the Chips Fund. This would introduce a structure as depicted below: the Chips JU would implement activities under the original KDT JU (also known as 'non-Initiative' activities) and activities under the Chips for Europe Initiative. The latter activities could be broken down in research & innovation activities and in capacity building activities. The original KDT activities are research & innovation activities. All research & innovation activities will be based on the Strategic Research and Innovation Agenda prepared by the industry associations. Horizon Europe would be the funding source for research & innovation activities, whereas the Digital Europe Programme would fund capacity building activities.

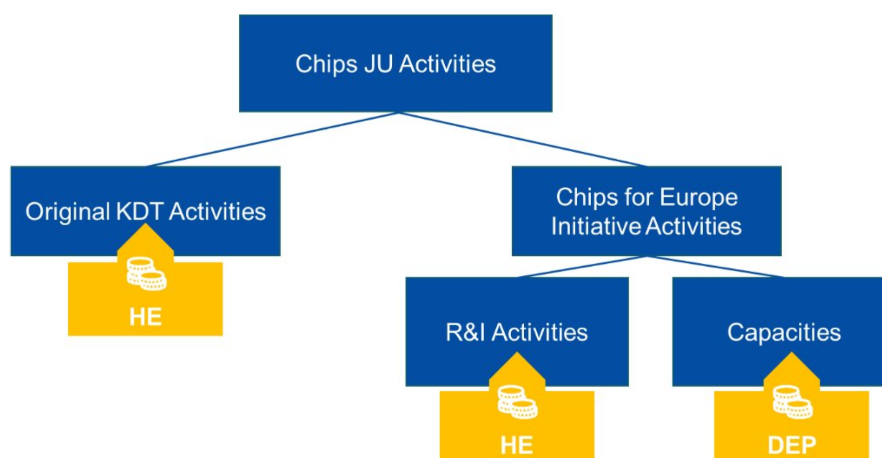


Figure 47. Overview of different activities under the Chips JU

The SBA amendment would introduce slightly changed decision making procedures but would not change the composition of the renamed **Chips Joint Undertaking's** Governing Board (GB) and Public Authorities Board (PAB). It would further extend the role of the PAB, by giving it the task to outline, before the work programme is defined in detail and adopted, the different parts of the work programme as shown above, including their corresponding expenditure estimates. Adoption of the work programmes and project selection would still be done by respectively the Governing Board and the Public Authorities Board, but both would act in different configurations for the Chips for Europe Initiative and the non-Initiative activities.

The **Governing Board**, which would still consist of representatives of participating states, private members, and the Commission, would continue being the main decision-making body of the Joint

[72] The Alliance consists of stakeholders from across the semiconductor value chain, such as RTOs and private companies, and is facilitated by the Commission (formally, the Commission is not a member of the Alliance). The overall objective of the Alliance is to identify current gaps in the production of microchips and the technology developments needed for companies and organisations to thrive. To this end, it will have a General Assembly and specialised working groups.

Undertaking. The GB has the overall responsibility for the strategic orientation and operations of the Joint Undertaking as well as their coherence with relevant Union objectives and policies. In a nutshell, it supervises the implementation of the Joint Undertaking's activities and adopts its work programmes.

The composition of the **PAB** would also remain unchanged; it would still consist of the relevant public authorities of the participating states (Member States and associated countries) and the Commission. The PAB would contribute to the drafting of the strategic research and innovation agenda (SRIA) and would provide input to the draft work programmes, which would later be adopted by the GB. The PAB would also approve the launch of calls for proposals and be responsible for the selection of projects on the basis of the ranking list prepared by the evaluation committee and decide on the allocation of public funding to selected proposals.

Finally, Article 171[73] of the SBA, as currently in force, provides a framework for the monitoring and evaluation of all Joint Undertakings set up in the SBA, including, the KDT Joint Undertaking. This provision will not be changed with the SBA amendment and it will continue applying to the proposed Chips Joint Undertaking. This framework ensures a continuous monitoring of the management and implementation of the activities of the Chips Joint Undertaking, in accordance with its financial rules, in order to ensure the highest impact, scientific excellence and the most effective and efficient use of resources.

Monitoring and reporting will include, amongst other, time-bound indicators for the purpose of reporting on the progress of the Chips Joint Undertaking's activities towards the achievement of its general, specific and operational objectives; information on synergies between the Chips Joint Undertaking's actions and national or regional initiatives and policies; information on quantitative and qualitative leverage effects; and information on measures to attract newcomers, particularly SMEs, higher education institutions and research organisations, and to expand collaborative networks.

To this end, the Commission will carry out an interim and a final evaluation of the Chips Joint Undertaking, which will feed into the Horizon Europe evaluations. These evaluations will examine how the Chips Joint Undertaking fulfils its mission and objectives as well as its European added value, effectiveness, efficiency, including its openness and transparency, the relevance of the activities pursued and their coherence and complementarity with relevant regional, national and Union policies, including synergies with other parts of Horizon Europe. These evaluations will also take into account the views of stakeholders, at both European and national level."

[73] Article 171 (Monitoring and evaluation) of the SBA (Council Regulation (EU) 2021/2085). See SBA link: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32021R2085

10. Budgetary Aspects

10.1 Investment

The European Chips Act is to be supported with an estimated overall level of policy-driven investment in excess of EUR 43 billion up to 2030[74]. The expectation is that this will attract similar levels of long-term private funding. The overall public investment will include EUR 11 billion for the Chips for Europe Initiative which targets technology leadership in research, design and manufacturing capacities up to 2030[75]. A key aim is to pool investment from the Union, private investors and the Member States to provide the critical mass of funding required. Additionally, underpinning this investment equity support will be provided to start-ups, scale-ups and other companies in the supply chain via a EUR 2 billion 'Chips Fund'. Together these should result in public and private investments exceeding EUR 15 billion.

Furthermore, loans from the EIB for the entire semiconductor ecosystem will be made available. At the Member State level additional support for the Chips for Europe Initiative may also come from national or regional funds and funding targeting microelectronics in recovery and resilience plans. Unused loan capacity under the Recovery and Resilience Facility can also be used by Member States to provide support. This complements activities such as the new IPCEI which will support cross-border innovative projects along the microelectronics value chain, including through the Recovery and Resilience Facility and Structural Funds. Additionally, there will also be support for setting up of large manufacturing facilities. Although the specific amount cannot be announced yet, it is expected that public investments by Member States, coming from Recovery and Resilience Plans, Cohesion Fund plans, national budgets etc. for purposes such as the IPCEI and large manufacturing projects, would total EUR 30 billion.

10.2 Breakdown of Funding Components

The budgetary construction of the Chips Act proposal is described in the **legislative and financial statement** (LFS) accompanying the proposed Chips Act.[76]

The EU budget will support the Chips for Europe Initiative with funding of **up to EUR 3.3 billion**, including EUR 1.65 billion via Horizon Europe and EUR 1.65 billion via the Digital Europe Programme. Out of this total amount, EUR 2.875 billion will be implemented through the Chips JU, EUR 125 million through InvestEU (against which the EIB group is expected to provide additional financing of up to EUR 125 million) and EUR 300 million through the European Innovation Council. This comes in addition to the budget already dedicated to activities in microelectronics planned for 2021-27 to reach almost EUR 5 billion.

- **Horizon Europe**: an amount of up to EUR 1.65 billion will be implemented under HE in favour of the Chips for Europe Initiative, including EUR 300 million under the European Innovation Council (EIC), and 500 million from the current EUR 1.8 billion dedicated to the Key Digital Technologies Joint Undertaking.

[74] Public investment and leveraged equity support.

[75] EUR 5.85 billion EU investment + EUR 5.3 billion MS investment.

[76] Financial details on the amendment of Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (for the Chips JU) are provided in the Legislative Financial Statement annexed to the Chips Act proposal.

- **Digital Europe Programme**: a new Specific Objective 6 is proposed for the purposes of the Chips for Europe Initiative. The Specific Objective 6 covers components a) to e) of Article 5 of the Chips Act[77] (see section below). A total of up to **EUR 1.65 billion** will be allocated to this new Specific Objective 6 of the programme, through reallocation from the existing objectives of the DEP, a contribution from the Connecting Europe Facility Programme (CEF)and from the unallocated margin of Heading 1 and decommitments from the HE programme.

  In order to compensate for the decommitments of Horizon Europe, the Commission proposes to make available again, for the benefit of the HE programme, a further amount of commitment appropriations over the period 2023-2027, resulting from total or partial non-implementation of projects belonging to that programme or its predecessor. This amount will be in addition to the EUR 500 million (in 2018 prices) already mentioned in the Joint Declaration by the European Parliament, the Council and the Commission on the re-use of decommitted funds in relation to the research programme.

[77] The 5 components are: (a) design capacities for integrated semiconductor technologies; (b) pilot lines for preparing innovative production, and testing and experimentation facilities; (c) advanced technology and engineering capacities for quantum chips; (d) a network of competence centres and skills development; and (e) 'Chips Fund' activities for access to debt financing and equity to start-ups, scale-ups, SMEs and other companies in the semiconductor value chain.

Budget implementation - the Chips Joint Undertaking

The Regulation 2021/2085 establishing the Joint Undertakings under Horizon Europe (Single Basic Act (SBA)) is amended and expanded to allow the Key Digital Technologies Undertaking (KDT JU), renamed as **Chips Joint Undertaking (Chips JU)** to implement most of the increased contribution from HE and contributions from DEP under the Specific Objective 6.

The components under the Chips for Europe Initiative listed in points (a) to (d) of Art. 5 of the Chips Act may be entrusted to the Chips JU and implemented in its work programme[133].

Article 128 of the proposed amendment to the SBA, as regards the Chips JU, indicates that the proposed Union financial contribution '*shall be up to* ***EUR 4.175 billion***'.

Most of the budget of the Initiative mentioned above (up to **EUR 1.65 billion from HE +** up to **1.65 billion from DEP**) will be channelled via the Chips JU, with the **exception** of:

- **EUR 125 million** of the Digital Europe Programme, which will be implemented under InvestEU, and
- **EUR 300 million** of the European Innovation Council (part of the Horizon Europe programme), which will be implemented by the EIC.

Finally, the budget of the current KDT JU (**EUR 1.3 billion**, given that EUR 500 million of the EUR 1.8 billion currently indicated in the SBA are earmarked for the Chips for Europe Initiative, as indicated above) will continue being part of the budget of the renamed Chips JU.

This leads to the total Union contribution of 'up to **EUR 4.175 billion**', of which EUR 1.525 billion from the Digital Europe Programme and EUR 2.65 billion from Horizon Europe. This leads to the following breakdown (in EUR billion):

	Chips for Europe Initiative	**Non-Initiative**	**Total**
Research & Innovation (Horizon Europe)	1.350	1.300	2.650
Capacity building (Digital Europe)	1.525	n.a.	1.525
Total	2.875	1.300	4.175

11. Application of the ‘one in, one out’ approach

The implementation of the Chips Act is expected to create no administrative cost for citizens and only a marginal administrative cost for businesses. The expected administrative cost for businesses relates primarily to the new monitoring and crisis response measures under the Pillar 3 of the Chips Act as outlined in Chapter 4 of the Proposal for a Regulation[78] and in Section 8.3 of this SWD. Pillar 2 “A Framework to ensure Security of Supply”, outlined in Section 8.2 of this SWD, while voluntary in nature, may incur administrative cost for businesses. However, these administrative costs would be non-significant. Pillar 1 “The Chips for Europe Initiative” of the Proposal for a Regulation, as outlined in Section 8.1, puts forward measures of a voluntary nature (e.g. applications for R&I support) and as such does not imply an administrative cost for businesses.

Under Pillar 2, the expected administrative costs would result from participation in the voluntary framework for “Integrated Production Facilities” and “Open EU Foundries”. Businesses would have to provide certain documentation, specified in Article 12, when applying for recognition of their project as either type of facility. However, it is expected that businesses would have this information available, as it is documentation typically required to receive financial support. Additionally, there might be further synergies in procedures if a business also seeks public support. The Commission’s monitoring of businesses recognised as “Integrated Production Facility” or “Open EU Foundry” may incur administrative costs for these businesses. This administrative cost would depend on the frequency and type of documentation required, but would be limited to companies voluntarily participating in the scheme, which in turn receive several benefits (see Section 8.2.2). Therefore, the incurred administrative cost may be considered as non-significant.

Under Pillar 3, a distinction must be made between the nature of the obligations deriving from the regular monitoring activities and the crisis response measures. Under Article 15 of the Proposal for a Regulation, Member States *shall invite* the main users of semiconductors and other relevant stakeholders to provide information regarding significant fluctuations in demand and known disruptions of their supply chain. The provision of such information would be voluntary. The administrative cost for businesses depends on many factors, such as the type of infrastructure needed, the format in which data would be delivered and the level of customisation needed, as well as on the frequency of the invitations for monitoring (monthly, bimonthly, or quarterly). With the information at hand and considering that a limited number of businesses, mostly large companies users and suppliers of chips, would be involved in the process, the administrative cost for providing information is considered marginal.

According to Article 20 of the Proposal for a Regulation, in case of the activation of the crisis stage, the Commission *shall request* representative businesses operating along the semiconductor supply chain to provide information about their production capabilities, production capacities, current primary disruptions and other existing data necessary to assess the nature of the semiconductor crisis or to identify and assess potential mitigation or emergency measures at national or Union level. Addressees of such information requests *shall* supply the requested information. The crisis stage would be activated in exceptional circumstances only, as defined in Article 18. The information that businesses would need to provide in case of a crisis would be of a similar nature and volume to the information that they are already collecting on a regular basis for various business practices, e.g. for

[78] COM(2022) 46. Proposal for a Regulation establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act). 08/02/2022

ensuring business continuity, and it is expected that businesses can benefit from solutions put in place in the context of the monitoring activities. Hence, the new legal obligation of sharing this information with the Commission in case of a crisis would not imply a significant administrative cost.

The details for implementation of the crisis response measures under Pillar 3 of the Proposal for a Regulation are still under negotiation with the Member States, as well as under consultation with the EU semiconductor industry. Even though at the present moment the administrative cost resulting from these measures is expected to be non-significant, an accurate estimation would only be possible once the discussions on the implementation are complete.

Overall, the Chips Act's new monitoring and crisis response measures are expected to bring important economic and social benefits by preventing and mitigating disruptions in the supply chain, avoiding market shocks and ensuring the availability of chips, especially for critical sectors. These expected benefits would justify the introduction of a marginal administrative cost for businesses.

12. What success looks like

Success will be measured against the achievement of objectives in an efficient and effective manner. The overarching objective of the EU Chips Act is set by the 2030 Digital Compass[79] and establishes that Europe will deliver 20% of semiconductors world production by 2030. The implementation of the Act in three pillars and correspondent initiatives would allow the follow up of specific objectives and the materialisation of the expected benefits and impacts.

The EU Chips Act will be considered successful if a gradual and tangible progress towards the following objectives can factually be confirmed within the time and resources planned:

- Strengthen EU research and technology leadership
- Address the skills shortage, attract new talent and support the emergence of a skilled workforce
- Reinforce the capacity of Europe for innovation in design, wafer manufacturing and packaging
- Establish a framework to increase substantially production capacity by 2030
- Develop an in-depth understanding of global semiconductor supply chains and enable the EU to take appropriate measures when necessary

[79] COM(2021)118. 2030 Digital Compass: the European way for the Digital Decade. 09/03/2021

Glossary

AI - Artificial Intelligence is used to give a computer or a robot controlled by a computer the ability to do tasks that are usually done by humans that require human intelligence or discernment.

ASICs - Application Specific Integrated Circuits are customed designed circuits for specific applications.

Back-end - Back end semiconductor manufacturing refers to the fabrication processes after all of the features/circuits have been created on the wafer

BiCMOS - BiPolar CMOS technology integrates two semiconductor technologies, those of the bipolar junction transistor and the CMOS (complementary metal-oxide-semiconductor) gate, in a single integrated circuit device.

CAD - Computer Aided Design is the use of computers to aid in the creation, modification, analysis, or optimization of a design. This increases the productivity of the designer, improves the quality of design, improves communications through documentation, and creates a database for manufacturing.

CAGR - Compound Annual Growth Rate is the mean annual growth rate of an investment over a specified period of time longer than one year.

CAPEX - Capital Expenditure

CEF - Connecting Europe Facility Programme is a European Union fund that supports infrastructure investments across the union in transport, energy and digital projects aimed at a greater connectivity between EU member states. It is operated through grants, financial guarantees and project bonds.

Chiplet – chiplet-based design is an approach whereby a single chip is broken down into multiple smaller chiplets and then "re-assembled" using advanced packaging solutions.

CMOS - Complementary Metal Oxide Semiconductors consists of a pair of semiconductors connected to a common secondary voltage such that they operate in opposite (complementary) fashion. CMOS is the predominant semiconductor technology.

CPUs – Central Processing Units are used within microprocessors to execute instructions.

CT - Computerised tomography scans use X-rays and a computer to create detailed images of the inside of the body.

DEP – The Digital Europe Programme is an EU programme that supports technological leadership.

DoD - Department of Defense

EAR - Export Administration Rules

ECG - An electrocardiogram is a test used to check the heart's rhythm and electrical activity.

ECIC - European Chips Infrastructure Consortia

ECSEL JU - Electronic Components and Systems for European Leadership Joint Undertaking is an EU driven, public private partnership, funding innovation in electronic components and systems.

EDA - Electronic Design Automation is a set of software tools for designing electronic systems such as integrated circuits and printed circuit boards. The tools work in a design flow that chip designers use to design and analyse entire semiconductor chips.

EDIHs - European Digital Innovation Hubs will function as “one-stop shops” that help companies dynamically respond to the digital challenges and become more competitive.

EIB - European Investment Bank

EMIB - Embedded Multi-Die Interconnect Bridge technology allows the use of silicon from different process nodes in the same package.

EUV - Extreme Ultraviolet Lithography is an optical lithography technology using a range of extreme ultraviolet (EUV) wavelengths to produce a pattern by exposing a reflective photomask to Ultra Violet light which gets reflected onto a substrate covered by photoresist. Chemicals are then used to etch the substrate along with other processes to create the chip die.

EV - Electric Vehicles use battery technology and one or more electric motors for propulsion.

FID - First Industrial Deployment

FOWLP - Fan-Out Wafer Level Packaging is an integrated circuit packaging technology, and an enhancement of standard wafer-level packaging solutions. It provides a smaller package footprint along with improved thermal and electrical performance compared to conventional packages. Additionally, it allows a higher number of contacts without increasing the die size.

FDSOI - Fully Depleted Silicon on Insulator is a planar process technology that delivers the benefits of reduced silicon geometries while simplifying the manufacturing process. FDSOI provides improved performance and low power.

FETs - F*ield-Effect Transistor*s use an electric field to control the flow of current in a semiconductor.

FinFETs - Fin Field-Effect Transistors are a multigate metal oxide semiconductor field effect transistor. They get their name from the fins formed on the silicon surface. FinFETs provide significantly faster switching times and higher current density than other planar CMOS technologies.

FOAK - First-Of-A-Kind (FOAK), to be introduced under the EU's Chips Act, would allow state aid funding to be used for "first-of-a-kind" production sites in Europe, as part of a larger goal of producing 20 percent of the world's semiconductors by 2030.

FPGAs - Field Programmable Gate Arrays provide programmable logic devices that can be programmed by the end user in the field.

FRAND - Fair, Reasonable and Non-Discriminatory

Front-end - the fabrication from a blank wafer to a completed wafer

GaaFET - Gate all around FET transistors use a modified transistor structure where the gate contacts the channel from all sides which enables continued scaling. GAA transistors offer better performance than FinFETs.

GaN - **Gallium Nitride (*GaN*)** is a material that can be used in the production of *semiconductor* power devices.

GB - Governing Board (ECSEL)

Gbps - Giga bits per second is a data transfer rate equivalent to one billion bits per second.

GDP - Gross Domestic Product

GDPR - General Data Protection Regulation

GHG - Green House Gas

GPUs – Graphics Processing Units are used in graphics rendering and acceleration, for instance in video processing and gaming applications.

Green Deal – The Green Deal, presented in December 2019, has the overarching objective that the EU should become the first climate neutral continent by 2050, resulting in a cleaner environment, more affordable energy, smarter transport, new jobs and an overall better quality of life.

HE - Horizon Europe supports intensive pre-competitive research, and technology development. This includes innovation in the area of materials and semiconductors.

HPC - High Perfomance Computing

IC - Integrated Circuits are a set of electronic circuits on one small flat piece of semiconductor material, usually silicon.

ICT - Information and Communications Technology is defined as a diverse set of technological tools and resources used to transmit, store, create, share or exchange information. Examples are laptops, routers, data servers, etc.

IDMs - Integrated Device Manufacturers are semiconductor companies which design, manufacture, and sell integrated circuit (IC) products.

IoT - The Internet of Things describes physical objects with sensors, processing ability, software, and other technologies that connect and exchange data with other devices and systems over the Internet or other communications networks.

IP - Intellectual Property blocks/cores are reusable units of logic or integrated circuit layout that are used in chip design that are the intellectual property of one party. IP cores can be licensed to another party or owned and used by a single party.

IPCEI - Important Projects of Common European Interest are large scale projects bringing together companies and research centres from different Member States to provide significant benefits to strategic EU goals (competitiveness, sustainable growth, societal challenges, value creation, …). In the semiconductor area there is an IPCEI on Microelectronics.

IPF - Integrated Production Facilities are vertically integrated semiconductor manufacturing facilities, which are involved in the front-end manufacturing as well as in the design of integrated circuits or the provision of back-end services, such as assembly, testing and packaging, or both.

IRDS - International Roadmap for Devices and Semiconductors is a set of predictions about likely developments in electronic devices and systems published by the IEEE.

JPA - Joint Procurement Agreements enable the Commission to organise collective procurement on behalf of participating Member States.

JU - Joint Undertakings complement the existing Horizon Europe framework by addressing global challenges and priorities that require critical mass and long-term vision. Joint undertakings enable the joint investment of tens of billions of euros by public and private actors, at EU and national level.

KDT - Key Digital Technologies

LEDs – Light Emitting Diodes are a semiconductor light source that emit light when current flows through them. Electrons in the semiconductor recombine with electron holes, releasing energy in the form of photons.

LiDAR - Light Detection and Ranging, is a remote sensing method that uses light in the form of a pulsed laser to measure distances.

Mbps - Megabyte per second is a unit of data transfer rate equal to 8,000,000 bits per second or 1,000,000 bytes per second.

MCU - Microprocessor Control Units direct the operation of other units within a processor by providing timing and control signals. It is the function of the microcomputer to execute programs which are stored in memory in the form of instructions and data.

MEMS - Micro-electromechanical Systems is a process technology used to create tiny integrated devices or systems that combine mechanical and electrical components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimetres.

ML - Machine Learning is an Artificial Intelligence approach which focuses on the use of data and algorithms to imitate the way that humans learn, gradually improving accuracy. ML algorithms are trained using three prominent methods: supervised learning, unsupervised learning, and reinforcement learning.

MRI - Magnetic resonance imaging is a medical imaging technique that uses a magnetic field to create detailed images of the organs and tissues in your body.

MS - Member States

NDA - Non-Disclosure Agreement is a legally binding contract that establishes a confidential relationship. The party or parties signing the agreement agree that sensitive information they may obtain will not be made available to any others.

Nm - Nanometres are a unit of length in the metric system, equal to one billionth of a metre. One nanometre can be expressed in scientific notation as 1×10^{-9} m, and as 1/1000000000 metres.

OEM - Original Equipment Manufacturers make systems or components that are used in another company's end product. Computer manufacturers, for example, commonly bundle or integrate OEM parts, such as processors and software, into the solutions they sell.

Open EU Foundries are semiconductor manufacturing facilities which dedicate at least a significant extent of their production capacity to produce chips according to the design of other companies, in particular fabless companies.

OSATs - Outsourced Semiconductor Assembly and Test companies provide third-party IC-packaging and test services.

PAB - Public Authorities Board (ECSEL)

PCB - Printed Circuit Boards have a laminated sandwich structure of conductive and insulating layers onto which chips are integrated to create electronic products.

PDK - Process Design Kits provide a set of files which are used within the semiconductor industry to model a fabrication process. The PDK is created by the foundry defining a certain technology variation for their processes. Foundry customers use this information in their design tools to design appropriate integrated circuits.

PPAC-E - Power, Performance, Area, Cost and Environmental impact

QT - Quantum Technologies are a class of technology that works by using the principles of quantum mechanics (the physics of sub-atomic particles), including quantum entanglement and quantum superposition.

RibbonFET is a new transistor architecture based on gate all around transistors, which Intel plans to start producing commercially in 2024.

RF - Radio Frequency is the oscillation rate of an alternating electric current or voltage, or magnetic/electric/electromagnetic field in the frequency range from around 20 kHz to around 300 GHz.

RISC-V - Reduced Instruction Set Computer -V is an open standard instruction set architecture that began in 2010 and is based on established reduced instruction set computer principles. Unlike most other ISA designs, RISC-V is provided under open source licenses that do not require fees to use.

RoHS – The Restriction of Hazardous Substances Directive 2002/95/EC, restricts the use of certain hazardous substances in electrical and electronic equipment.

RTO - Research and Technology Organisations are specialised knowledge organisations dedicated to the development and transfer of science and technology for the benefit of the economy and society.

SaaS - Software as a Service is a software licensing and delivery model in which software is licensed on a subscription basis and is centrally hosted.

SBA - Single Basic Act

SiC - Silicon Carbide offers advantages over silicon when used in semiconductor technology, including a higher critical breakdown field, which means a voltage rating can be maintained while still reducing the thickness of the device and a wider bandgap, which leads to lower leakage current at relatively high temperatures. This is important for power electronics and is likely to have a big impact on areas such as electromobility.

SIMD - Single Input Multiple Data processing can process multiple data values using a single instruction. One instruction can therefore do the work of many which is very powerful for computations in areas such as media data.

SiP - System-in-Package integration integrates a number of integrated circuits in one or more chip carrier packages that may be stacked using package on package. SiPs are commonly used in mobile phones, digital music players, etc.

SME - Small and Medium Enterprises are defined by the EC as having less than 250 staff, a turnover of less than EUR 50 million and a balance sheet of less than EUR 43 million. Within this definition there are also Small and Micro Companies with less staff and turnover.

SoC - System on Chips integrate all or most components of a computer or other electronic system in a single device.

SOI - Silicon On Insulator fabricates silicon semiconductor devices in a layered silicon–insulator–silicon substrate to reduce parasitic capacitance within the device resulting in an improvement in performance.

TFEU - Treaty on the Functioning of the European Union

TPU - Tensor Processing Units are application specific integrated circuits developed by Google specifically as an AI accelerator for neural network implementation in machine learning.

VC - Venture Capital

3D Stacking is a three-dimensional integrated circuit approach where silicon wafers or dies are interconnected vertically by using through-silicon vias (TSVs) or via Cu-Cu connections, so that they

behave as a single device. This results in performance improvements at reduced power and smaller footprint than conventional two-dimensional processes.

“III-V materials” refers to compound semiconductor materials combining elements of the group III and V of the periodic table. Gallium-nitride (GaN) and indium-phosphide (InP) are examples of III-V materials.

4G - 4G stands for “fourth generation” and refers to mobile network technology that enables 4G compatible phones to connect to the internet.

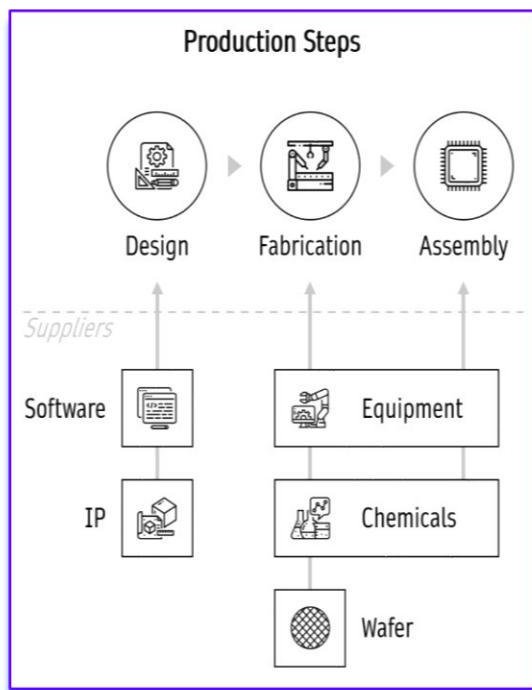
5G - 5G stands for “fifth generation” and this network offers low latency, high datarate communications enabling the connection of people, machines, objects, and devices.

6G - 6G stands for “sixth generation” and is currently under development for wireless communications technologies supporting cellular data networks. This successor to 5G will be significantly faster opening up new concepts such as the “metaverse”.

Annex 1. Introduction to Semiconductors

Semiconductors are the material basis for chips[80] embedded in virtually every technology product today. Chips are miniaturised physical devices that can capture, store, process and act on data. They come in many families - some of which are shown in the box below.

Chips are also an enabler for emerging technologies, such as artificial intelligence, quantum computing, and autonomous and electric vehicles. A recent report by the White House[81] refers to semiconductor chips as being "*the 'DNA' of technology*".



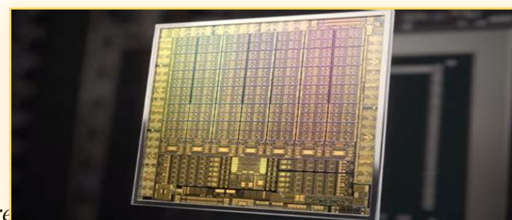
The active component of a chip is a transistor - an electronically controlled switch.

Since the 1960s, the business of chip production has been driven by doubling the amount of transistors in a given area of semiconductor - and hence doubling the computing power without cost - every eighteen months[82].

It is characterised by rapid technological change fuelled by constant research and development (R&D) at all stages of the value chain: from the software and intellectual property[83] that support the process of chip design, to the materials (wafers and chemicals) and equipment that support the processes of fabrication, and subsequent assembly, test and packaging of the chip. Over the last 20 years, the annual R&D expenditure as a percentage of revenues has been consistently between 15 and 20%.

This elaborate process translates to a complex and global supply chain, high capital investment costs with large economies of scale and significant market concentration.

Today, leading-edge fabs are equipped with the most modern process technologies that enable transistors to be printed with a precision of 5 nm[84]. Chips such as GPUs[85] designed for very compute-intensive applications have around



Nvidia's Ampere ... nm GPU - it has 28 billion transistors

[80] Often referred to as integrated circuits or ICs.

[81] *Building Resilient Supply Chains, revitalising American Manufacturing, and fostering Broad-based Growth*, June 2021.

[82] Referred to as Moore's Law, dating from 1965 when a chip had just 64 transistors. It's why an iPad today has more processing power than a (refrigerator-sized) Cray supercomputer in 1990. More in Annex 3.

[83] Because of the complexity of designing chips with millions or even billions of transistors, chip designers license intellectual property or IP blocks (essentially basic functional building blocks or architectures).

[84] In semiconductor manufacturing, the process technology (or process node) has traditionally been correlated with the transistor dimension. It is measured in nanometres: 1 nm or 1 nanometre = 1 billionth of a meter. Smaller process nodes produce smaller transistors, which are faster and more power efficient. The state-of-the-art process node is 5 nm today, with 3 nm in pre-production and 2 nm under development. Only TSMC and Samsung, are producing at 5 nm (Intel is struggling with 7 nm).

[85] Graphics Processing Units (GPUs) are used to accelerate computing processes, for graphics rendering in gaming and are increasingly important for artificial intelligence due to their capability to process large data volumes with high efficiency. Nvidia developed GPU technology and is currently the market leader.

50 billion transistors. The cost of building a leading-edge fab can be up to EUR 20 billion; designing and developing such a complex chip can be in the range of EUR 1 billion[86].

Given the cost of building a modern fab and developing new process technology, the fab production line needs to be kept full. The volume required for cost-effective manufacturing is so high[87] that very few semiconductor companies can fill their own fab even if they could afford to build it.

This has transformed the business dramatically. Previously dominated by Integrated Device Manufacturers (IDMs) who design their own chips and have their own facilities for fabrication and assembly, today most companies run their businesses based on "fabless" or "fab-lite" models whereby they outsource all or some of their fabrication to foundries[88].

Further, only a small handful of foundries have the financial and commercial muscle to build leading-edge fabs, driven by microprocessors for computers and mobile handsets - high volume businesses that need the highest possible performance and the lowest possible power.

The other part of the foundry business is not focused on the leading edge but on designs for sensors, power management, and so on. For these designs, the state-of-the-art process today is 65 nm and so does not require the most leading-edge fab.

[86] https://www.extremetech.com/computing/272096-3nm-process-node

[87] At least 50,000 wafers per month for the most modern fabs. Wafers are generally 300mm in diameter. One such wafer would hold 150 (giant) chips of 20x20mm. This would equate to 7.5 million chips per month.

[88] TSMC is the world's largest foundry with revenues of USD 34 billion. Intel, nowadays an IDM, designs and fabricates its own chips, but has recently announced its intention to enter the foundry business.