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NOTE

From:	General Secretariat of the Council
To:	Delegations
Subject:	Proposal for a REGULATION OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL on a framework of measures for strengthening the Union's semiconductor ecosystem, repealing Regulation (EU) 2023/1781 (Chips Act 2.0) - Presidency compromise text

In view of the upcoming meeting of the Working Party on Competitiveness and Growth (Industry) on 7 October July 2026, delegations will find in Annex to this note a marked version of the Presidency compromise text on Pillars I and II of the proposed Regulation. Changes in comparison to the Commission proposal, document ST 10094/26 + ADD1, are marked in **bold** for additions and in ~~strikethrough~~ for deletions.

ANNEX

2026/0139 (COD)

Proposal for a

REGULATION OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL

on a framework of measures for strengthening the Union's semiconductor ecosystem~~,~~ and repealing Regulation (EU) 2023/1781 (Chips Act 2.0)

(Text with EEA relevance)

THE EUROPEAN PARLIAMENT AND THE COUNCIL OF THE EUROPEAN UNION,

Having regard to the Treaty on the Functioning of the European Union, and in particular Article 173(3) and Article 114 thereof,

Having regard to the proposal from the European Commission,

After transmission of the draft legislative act to the national parliaments,

Having regard to the opinion of the European Economic and Social Committee[1],

Having regard to the opinion of the Committee of the Regions[2],

Acting in accordance with the ordinary legislative procedure,

Whereas:

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1 OJ C , , p. .
2 OJ C , , p. .

(1) Regulation (EU) 2023/1781 of the European Parliament and of the Council[3] establishing a framework of measures for strengthening Europe's semiconductor ecosystem and amending Regulation (EU) 2021/694 (Chips Act) established a comprehensive framework at Union level to support the semiconductor ecosystem, with a view to strengthening the Union's technological capacity, enhancing resilience and ensuring security of supply.

(2) The evaluation[4] of the Regulation (EU) 2023/1781 shows that it has enabled the mobilisation of significant public and private investment, the deployment of advanced infrastructures and the establishment of coordination and crisis preparedness mechanisms, thereby contributing to improved cooperation across Member States and to the functioning of the internal market. The evaluation has shown that Regulation (EU) 2023/1781 has served as a catalyst for a coordinated Union approach to semiconductors, strengthening research and innovation capacities, proving access to technological infrastructures, putting in place a framework for manufacturing capacity, as well as a crisis and response mechanism to anticipate potential disruptions. At the same time, the evaluation has identified structural shortcomings and persisting challenges that limit its effectiveness in addressing evolving industrial and economic needs.

(3) While the framework established by Regulation (EU) 2023/1781 has proven effective in supporting innovation and early-stage capacity, the transition from technological development to large-scale industrial deployment remains at an early stage. Long investment cycles, structural dependencies in critical segments of the value chain, and constraints in scaling up production continue to affect the Union's capacity to achieve a resilient and competitive semiconductor ecosystem.

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[3] Regulation (EU) 2023/1781 of the European Parliament and of the Council of 13 September 2023 establishing a framework of measures for strengthening Europe's semiconductor ecosystem and amending Regulation (EU) 2021/694 (Chips Act) (OJ L 229, 18.9.2023, p. 1, ELI: http://data.europa.eu/eli/reg/2023/1781/oj).

[4] [reference to the published evaluation report to be added]

PUBLIC

(4) In addition, the evaluation has shown that limited availability of private capital, in particular for later-stage financing, and structural features of financial markets constrain the growth and scaling of Union semiconductor undertakings. At the same time, fragmentation of demand across industrial sectors, limited market scale, and insufficient coordination among purchasers reduce the commercial viability of manufacturing investments **across the semiconductor value chain** and risk underutilisation of emerging capacities.

(5) Moreover, the semiconductor sector has become a cornerstone of the Union's economic stability, technological sovereignty, and security. The accelerating integration of advanced digital technologies, most notably artificial intelligence (AI), has significantly increased global demand for ~~semiconductors~~**chips**, while simultaneously intensifying competition across international markets. Those developments have exposed structural vulnerabilities in the Union's semiconductor supply chains, including dependencies on limited external suppliers, insufficient domestic production capacity, and fragmentation across Member States.

(6) The growing prominence of AI applications, in particular, has led to a surge in demand for highly specialized chips, such as advanced logic and memory ~~semiconductors~~**chips**, which are critical for training and deploying complex AI models. This trend is expected to continue, amplifying existing supply-demand imbalances and placing additional strain on already fragile global supply chains. At the same time, geopolitical tensions, export restrictions, and disruptions linked to global crises have further underscored the risks associated with excessive reliance on third country manufacturing and limited diversification.

(7) In light of those developments, it is necessary to reinforce and complement the framework established by Regulation (EU) 2023/1781 in order to support the transition from innovation to industrial scale, to enhance resilience and economic security, and to ensure the effective functioning of the internal market. Therefore, Regulation (EU) 2023/1781 should be repealed and replaced by this Regulation.

PUBLIC

(8) Since this Regulation reinforces and complements the framework established by Regulation (EU) 2023/1781 without altering its fundamental objectives, the legal bases underpinning that framework remain unchanged.

(9) Therefore, this Regulation should also be based on Article 173(3) of the Treaty on the Functioning of the European Union (TFEU) in order to allow the Union to take measures to further maintain and build capacity and strengthen its semiconductor ecosystem. Those measures should not entail the harmonisation of national laws and regulations. In that regard, the Union should reinforce the competitiveness and resilience of the semiconductor technological and industrial base, whilst strengthening the innovation capacity of its semiconductor ecosystem across the Union, reducing dependence on a limited number of third-country undertakings and geographies, and strengthening its capacity to design and produce, package, reuse and recycle advanced ~~semiconductors~~**chips**. The Chips for Europe Initiative first established by Regulation (EU) 2023/1781 should keep supporting those aims under this Regulation by further stepping up efforts beyond bridging the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation, and by ensuring the effective translation of such capabilities into industrial-scale production and market deployment within the Union. The Chips for Europe Initiative 2.0 should continue promoting capacity building to enable design, production and systems integration in next-generation ~~semiconductor~~**chip** technologies, and should continue supporting collaboration among key players across the Union, strengthening the Union's semiconductor supply and value chains, serving key industrial sectors and creating new markets.

PUBLIC

(10) In addition, and in order to ensure the effective functioning of the internal market, this Regulation should contribute to establishing a coherent Union framework approximating certain conditions and coordination mechanisms, in accordance with Article 114 TFEU. Such a framework is necessary to prevent obstacles to the functioning of the internal market, reduce fragmentation and ensure a consistent and effective response to supply chain risks, while remaining consistent with Union law and international obligations. This is particularly critical taking into account that semiconductors are a foundational technology underpinning a wide range of economic activities and critical infrastructures across the Union. In a context of heightened geopolitical tensions, strategic global competition and increasing economic security considerations, the semiconductor ecosystem has become a key factor for the stability and functioning of the internal market. The semiconductor sector is characterised by complex cross-border interdependencies across the value chain, with highly specialised activities concentrated in different geographies, while downstream user industries are widely distributed across the Union. Those characteristics mean that disruptions, restrictions or distortions affecting semiconductor supply chains are likely to have significant cross-border effects and to impact the functioning of the internal market. Divergent national measures aimed at addressing such risks may create fragmentation, distort competition and undermine the level playing field within the internal market, particularly given the integrated nature of production and distribution networks. Therefore, the objectives of ensuring the resilience, security and proper functioning of semiconductor supply chains within the Union cannot be sufficiently achieved by the Member States acting alone, but can be better achieved at Union level, by reason of their scale and cross-border effects.

PUBLIC

(11) The achievement of those objectives should continue being supported by the European Semiconductor Board, composed of representatives of the Member States and chaired by the Commission, to facilitate a smooth, effective, and harmonised implementation of this Regulation, cooperation, and the exchange of information. The European Semiconductor Board should provide advice to and assist the Commission on specific questions, including the consistent implementation of this Regulation, facilitating cooperation among Member States, and exchanging information on issues relating to this Regulation. The European Semiconductor Board should also advise the Commission on international cooperation related to semiconductors, including strategic partnerships on semiconductors and on information gathering tasks. Meetings may include different subgroups.

(12) Given the globalised nature of the semiconductor supply chain, international cooperation with third countries is an important element to achieve resilience of the Union's semiconductor ecosystem. The actions taken under this Regulation should also enable the Union to play a stronger role, as a centre of excellence, in a better functioning global, interdependent semiconductor ecosystem. Where relevant, the views of the Industrial Alliance for Semiconductors[5], which takes over the operations of the– Industrial Alliance on Processors and Semiconductor Technologies, and of other stakeholders should be considered. In accordance with international obligations, the Union and Member States could engage, including diplomatically, with international strategic partners that have advantages in the semiconductor industry, with a view to seeking solutions to strengthen the security of supply and to address future disruptions of the semiconductor supply chain, such as those resulting from third-country export restrictions, and to identify the availability of raw materials and intermediate products. The Commission and Member States should coordinate their international efforts, notably with support of the European Semiconductor Board. This may involve, where appropriate, coordination in relevant international fora, concluding investment and trade agreements, or other diplomatic efforts or engagement with relevant stakeholders. **Such cooperation should support the Union's open technological sovereignty, the development of durable and resilient value chains and the reduction of excessive dependencies and should include an assessment of technological security risks.**

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5 Terms of Reference - https://ec.europa.eu/newsroom/dae/redirection/document/78326

(13) Strengthening the Union's critical infrastructure, security, industrial base and technological leadership requires secure and reliable access to both leading-edge and mainstream ~~semiconductor~~**chip** technologies, including processors, memory, analogue, power, sensor, radiofrequency and connectivity chips, which are essential for future-proofing strategic sectors such as energy, defence, automotive, aviation, telecommunications, healthcare, cloud computing, and industrial automation. The Union possesses strong capabilities across a broad range of mature nodes, including in automotive-grade, power-efficient and secure chips, and should continue to reinforce its competitiveness, resilience, and strategic autonomy throughout the semiconductor value chain.

(13a) For the purposes of this Regulation, the term 'chip' should be understood broadly as referring to a finished device resulting from semiconductor manufacturing, irrespective of the technology, material or function concerned, while 'semiconductor' should be used where referring to the underlying technology, industry, ecosystem or value chain. The concept of 'quantum chip' should be technology-neutral and encompass chip-level devices providing quantum functionality, including where the relevant quantum states are generated, confined or maintained outside the chip or its substrate. It should not extend to the broader quantum systems or networks in which such devices are incorporated, or to external equipment necessary for their operation.

PUBLIC

(14) The semiconductor industry entails substantial investment requirements, both for research, development and innovation activities and for the construction of cutting-edge facilities dedicated to testing and validation in support of industrial-scale production. Those cost-intensive characteristics have a direct bearing on the Union's capacity to compete and innovate, and affect the security of supply and overall resilience of its semiconductor ecosystem. At the same time, the Union's competitiveness and resilience depend on the continued availability and development of mainstream and mature ~~semiconductor~~**chip** technologies, including analogue, power, sensor, connectivity, automotive-grade and aeronautical-grade chips, which remain indispensable across strategic industrial value chains and critical infrastructures. In the current context of increased global competition, geopolitical tensions, and structural supply chain vulnerabilities, semiconductors have become a strategic asset underpinning the Union's economic security, technological leadership, and industrial resilience. In light of the lessons learnt from past shortages and supply chain disruptions in the Union and worldwide, as well as export restrictions or regulatory actions by third countries and the rapid evolution of technology challenges and innovation cycles affecting the semiconductor value chain, it is necessary to reinforce the Union's existing strengths, including its leading position in several mainstream semiconductor segments, thus increasing market uptake, competitiveness, resilience, research and innovation capacity by further reinforcing the Chips for Europe Initiative.

(15) The enhanced Chips for Europe Initiative 2.0 should take into account the experience already gained through the implementation of the Chips for Europe Initiative in order to continue and reinforce it with a view to addressing remaining structural weaknesses and to responding to emerging strategic needs. In particular, it is necessary to step up efforts to ensure that the Union's advanced research and innovation capabilities effectively translate into industrial deployment, scale-up and production at commercial scale within the Union.

PUBLIC

(16) Member States are primarily responsible for sustaining a strong Union industrial, competitive, sustainable and innovative base. However, the nature and scale of the research and innovation challenges in semiconductors requires action to be taken collaboratively at Union level. In order to equip the Union with the ~~semiconductor~~**chip** technology research and innovation capacities needed to maintain the leading role of its research and industrial investments at the leading edge and building on the experience gained and lessons learnt from the implementation of the Chips for Europe Initiative, it is necessary to further strengthen and extend those capacities to ensure their effective industrial deployment, scale-up, and production at commercial scale within the Union. To this end, the Union and Member States should continue coordinating their efforts and co-invest.

(17) In light of increased global competition, geopolitical tensions, and the risk of disruptions of the semiconductor supply chain, including those arising from regulatory measures adopted by third countries that may affect access to critical ~~semiconductor~~**chip** technologies and related inputs, reinforcing the Union's capacity to develop**, design, package, test**, produce, and deploy such technologies within its territory has become a strategic priority for the Union's competitiveness, economic security, and technological sovereignty, as highlighted in the report by Mario Draghi entitled 'The future of European competitiveness'. These challenges of the Union's semiconductor ecosystem call for the achievement of large-scale capacity and require a collective effort by Member States, with the Union supporting the development and deployment of large-scale capacity across the full innovation and industrial value chain, including pilot lines, manufacturing scale-up, and commercial deployment, thereby ensuring the effective translation of research excellence into industrial leadership and sustainable production capacity within the Union.

(18) As concluded in the evaluation of Regulation (EU) 2023/1781, the instruments put in place by the Chips for Europe Initiative provided for by that Regulation, namely the design platform, pilot lines, quantum chips pilots, and the diffusion of knowledge, the EU Chips Skills Academy under the Alliances for Sectoral Cooperation on Skills and the Pact for Skills, and competences for the benefit of the entire semiconductor ecosystem are fit for purpose and should continue being supported under this Regulation. Those efforts should also contribute to the Union's broader objective of strengthening its long-term competitiveness, innovation capacity, and industrial base, including through synergies with future Union programmes supporting research and innovation and industrial deployment, such as the proposed[6] successor framework programme to Horizon Europe – the Framework Programme for Research and Innovation established by Regulation (EU) 2021/695 of the European Parliament and of the Council[7] (Horizon Europe) (FP10), and the proposed European Competitiveness Fund[8], while the Chips for Europe Initiative 2.0 should throughout all components and actions, to the extent possible, mainstream and maximise the benefits of the application of ~~semiconductor~~**chip** technologies as powerful enablers, for instance, for the sustainability transition that can lead to new products and more efficient, effective, clean, and durable use of resources, including energy and materials necessary for the production and whole lifecycle use of ~~semiconductors~~**chips, taking into account the durability, recoverability, reuse and recycling of materials, devices and modules and their environmental impact throughout their period of use.. Synergies with national semiconductor strategies and programmes of Member States should also be encouraged in order to maximise the impact of public investments and**

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6 Proposal for a regulation of the European Parliament and of the Council establishing Horizon Europe, the Framework Programme for Research and Innovation, for the period 2028-2034 laying down its rules for participation and dissemination, and repealing Regulation (EU) 2021/695

7 Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013 (OJ L 170, 12.5.2021, p. 1, ELI: http://data.europa.eu/eli/reg/2021/695/oj).

8 Proposal for a regulation of the European Parliament and of the Council on establishing the European Competitiveness Fund ('ECF'), including the specific programme for defence research and innovation activities, repealing Regulations (EU) 2021/522, (EU) 2021/694, (EU) 2021/697, (EU) 2021/783, repealing provisions of Regulations (EU) 2021/696, (EU) 2023/588, and amending Regulation (EU) [EDIP]

strengthen the participation of all Member States in the European semiconductor ecosystem.

(19) In order to achieve its general objective and address both the supply and demand side challenges of the current semiconductor ecosystem, and building on the experience gained and lessons learnt from the implementation of Regulation (EU) 2023/1781, which demonstrated the continued need to strengthen the Union's capacity not only in research and innovation but also in industrial deployment and manufacturing scale-up, the Chips for Europe Initiative 2.0 should keep supporting and further enhancing the five operational objectives put in place under Regulation (EU) 2023/1781. It should also introduce a new operational objective aimed at strengthening the Union's capabilities in photonic technologies and support 'grand challenges' as instruments to support large-scale, cross-sectoral initiatives addressing major technological and industrial challenges of strategic relevance for the Union. **Across its activities, including operational objectives and grand challenges, the Chips for Europe Initiative 2.0 should be implemented in close coordination with relevant initiatives, in particular those set up under the Cloud and AI Development Act and the European High-Performance Computing Joint Undertaking. Such coordination should help align investments in chip technologies and manufacturing capacities with the evolving needs of key downstream markets, in particular cloud, artificial intelligence and high-performance computing, while promoting coherence, complementarity and simplification and avoiding fragmentation across Union programmes and initiatives.** The primary implementation of the Chips for Europe Initiative 2.0 should continue being entrusted to the Chips Joint Undertaking and, where applicable, to the joint undertaking or any other similar entity or initiative succeeding it established by Union law under a subsequent Multiannual Financial Framework.

PUBLIC

(19a) **The Chips Joint Undertaking's implementation of operational objectives 1 to 5 of the Chips for Europe Initiative 2.0 and its grand challenges should follow the Joint Undertaking's established governance arrangements. This means that before the work programme is prepared, the Public Authorities Board, composed for this purpose only of the Commission and Member States, should, taking into account, where appropriate, the advice of the European Semiconductor Board and relevant stakeholders, outline the specific parts and relevant subsections of the work programme and their corresponding expenditure estimates, thereby providing strategic guidance on the priorities to be pursued. On the basis of that outline and the Strategic Research and Innovation Agenda, the Chips Joint Undertaking's Governing Board should adopt the work programme, including the calls and topics implementing the operational objectives and grand challenges. The applicable voting configurations in the Governing Board should ensure a decisive role for the Member States and the Commission in decisions concerning the implementation of the Chips for Europe Initiative 2.0.**

(19b) **Following the adoption of the work programme and the evaluation of proposals by independent experts in accordance with the rules of the relevant Union funding programme, the Public Authorities Board will select proposals for funding on the basis of the resulting ranking and the available Union and national funding. The governance arrangements of the Chips Joint Undertaking should preserve the ability of each Member State to determine the use of its own national financial contribution, ensuring that no Member State is required to provide national funding to beneficiaries established in its territory without its agreement. Actions implementing both the Chips for Europe Initiative 2.0 and other research and innovation activities of the Chips Joint Undertaking should be subject to the rules of the relevant Union funding programmes, thereby ensuring that calls are open to entities across the Union, subject, where justified in particular on security grounds, to limitations on participation provided for under those rules. In line with Programme rules, the design and selection of actions should also foster cross-border cooperation and an appropriate geographical balance across the Union.**

PUBLIC

(20) ~~First~~**Regarding its content**, the Chips for Europe Initiative 2.0 should **first** reinforce the Union's design capacity. To that end, it should keep supporting the virtual design platform set up under the Chips for Europe Initiative to connect the communities of design houses, start-ups, **scale-ups,** small and medium-sized enterprises (SMEs) and IP and tool suppliers and research and ~~technology~~**knowledge-dissemination** organisations to provide virtual prototype solutions based on co-development of technology, and to facilitate the transition from design to industrial production and commercial deployment within the Union.

(21) Second, in order to provide the basis for strengthening the security of supply and the Union's semiconductor ecosystem, the Chips for Europe Initiative 2.0 should keep supporting the enhancement of existing and development of new advanced pilot lines to enable development and deployment of cutting-edge ~~semiconductor~~**chip** technologies and next-generation ~~semiconductor~~**chip** technologies. The pilot lines should provide industry with a facility to test, experiment, and validate ~~semiconductor~~**chip** technologies as well as system design concepts**, including cybersecurity and security-by-design principles**, while reducing environmental impacts as much as possible, in order to accelerate their transition to industrial-scale ~~semiconductor~~**chip** manufacturing within the Union. Investments from the Union, alongside with Member States and the private sector, in pilot lines remain necessary to address persistent structural challenges and market failures, including insufficient availability of industrial-scale testing, validation, and ~~semiconductor~~**chip** manufacturing scale-up capacities in the Union, which continue to hinder innovation, industrial deployment, and global competitiveness.

(22) Third, in order to accelerate the innovative development of quantum chips and associated ~~semiconductor~~**chip** technologies, including those based on semiconductor material or integrated with photonics, conducive to the development of the semiconductor sector, the Chips for Europe Initiative 2.0 should support actions, including on design libraries for quantum chips, pilot lines **and packaging, including advanced packaging,** for building quantum chips and facilities for testing and validating quantum chips produced by the pilot lines with a view to enabling their industrial deployment and strengthening the Union's technological leadership in emerging ~~semiconductor~~**chip** technologies.

PUBLIC

(23) Fourth, in order to promote the use of ~~semiconductor~~**chip** technologies, to provide access to design and pilot line facilities, and to address skills gaps across the Union, the Chips for Europe Initiative 2.0 should continue providing Member States with the possibility to support at least one competence centre on semiconductors in each Member State, by enhancing existing centres or creating new facilities. **Such competence centres should continue to contribute to the strengthening of national semiconductor ecosystems, support skills development and technology transfer, and facilitate their integration into European semiconductor value chains.**

(24) Fifth, photonics and photonic integrated circuits are key enabling technologies for a wide range of strategic sectors, including telecommunications, data centres, artificial intelligence, sensing, healthcare, automotive, aeronautical and quantum technologies. They enable high-speed data transmission, energy-efficient processing, and advanced sensing capabilities, and are therefore critical to the Union's technological leadership, competitiveness, and security of supply. The Union has established strong research and innovation capabilities and holds leading positions in several segments of the photonics value chain. However, further efforts are needed to strengthen the Union's capacity to design, prototype, industrialise, ~~and~~ manufacture**, test and package** photonic integrated circuits and associated photonic semiconductor technologies at scale. To advance technology development in photonics and photonic integrated circuits, it is therefore necessary to support the development of design libraries and design tools, strengthen production technologies and material platforms, and reinforce pilot lines and open-access manufacturing facilities across multiple material platforms. Those actions should facilitate prototyping, testing, validation and industrial uptake, including through advanced integration and packaging technologies, and contribute to strengthening the Union's photonics ecosystem, enhancing its technological sovereignty, and accelerating the industrial deployment of innovative photonic technologies across the Union.

PUBLIC

(25) Sixth, the Commission should continue supporting the 'Chips Fund', that is to say, a dedicated semiconductor investment facility designed to strengthen the European semiconductor ecosystem by supporting start-ups, scale-ups, ~~and~~ SMEs **and small mid-caps,** proposing both equity and debt solutions, including a blending facility under the InvestEU Fund established by Regulation (EU) 2021/523 of the European Parliament and of the Council[9], and, if applicable, any other relevant investment scheme ~~under the Multiannual Financial Framework 2028-2034~~, in close cooperation with the European Investment Bank Group and together with other implementing partners such as national promotional banks and institutions**. To increase effectiveness, those activities should coordinate with similar instruments and support mechanism provided by Member States**. The Chips Fund activities should support the development of a dynamic and resilient semiconductor ecosystem by providing opportunities for increased availability of funds to support the growth of start-ups and SMEs as well as investments across the semiconductor value chain, including for other companies in the semiconductor value chain. In this regard, support and clear guidance should be provided~~, in particular to SMEs,~~ with the aim of assisting them in the application process. In that context, the European Innovation Council is expected to provide further dedicated support through grants and equity investments to high risk, market creating innovators.

[9] Regulation (EU) 2021/523 of the European Parliament and of the Council of 24 March 2021 establishing the InvestEU Programme and amending Regulation (EU) 2015/1017 (OJ L 107, 26.3.2021, p. 30, ELI: http://data.europa.eu/eli/reg/2021/523/oj).

(26) In order to further strengthen the Union's technological leadership and industrial competitiveness in semiconductors, it is appropriate to introduce the concept of 'grand challenges' as part of the Chips for Europe Initiative 2.0. Those grand challenges should focus on the development, integration and industrial deployment of promising and critical ~~semiconductor~~**chip** and related technologies of key importance for the Union. Grand challenges should support advanced research and development activities aimed at enabling the next generation of ~~semiconductor~~**chip** technologies, including those underpinning AI, cloud, data centres and edge infrastructures, with a particular focus on enhancing energy efficiency, securing capacities in leading-edge technologies and reinforcing the Union's manufacturing strengths. They should also address key technological roadblocks, including challenges related to miniaturisation, energy efficiency, sustainability, heterogeneous integration, **advanced packaging,** security, reliability and manufacturability. In order to maximise their impact, grand challenges should contribute to strengthening the semiconductor ecosystem across the Union by fostering collaboration along the semiconductor value chain, including with relevant vertical sectors. In particular, they should support structured cooperation between semiconductor developers**, research and knowledge-dissemination organisation** and user industries, with a view to achieving a competitive edge in applications critical for the Union's technological sovereignty and industrial base. Finally, grand challenges should further ensure the integration and alignment of efforts across existing infrastructures, including pilot lines, and promote their orientation towards industrial use. They should facilitate the transfer, maturation and uptake of technologies developed under the Chips for Europe Initiative 2.0, including through activities related to prototyping, testing, validation, demonstration, initial industrial deployment and integration into production environments.

PUBLIC

(27) Competence centres should contribute to maintaining the Union's lead with regard to chip research, development and innovation and design capabilities. The promotion of human potential and skills through education in science, technology, engineering and mathematics subjects up to the postdoctoral level is crucial for achieving that objective. In particular, competence centres should provide services to the semiconductor stakeholders, including start-ups and SMEs. Examples include facilitating access to pilot lines and to the virtual design platform, providing training and skills development, **supporting technology transfer and industrial uptake of research results,** support to finding investors, making use of existing local competencies or reaching out to ~~the~~ relevant ~~verticals~~**industrial sectors**. The services should be provided on an open, transparent and non-discriminatory basis. Each competence centre should connect and be part of the European network of competence centres in semiconductors and should act as an access point to other nodes of the network. In that regard, synergies with existing similar structures, such as European Digital Innovation Hubs set up under the Digital Europe Programme established by Regulation (EU) 2021/694 of the European Parliament and of the Council[10], should be maximised. For example, Member States could designate an existing European Digital Innovation Hub focused on semiconductors as a competence centre for the purposes of this Regulation, provided that the prohibition of double financing is not breached.

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10 Regulation (EU) 2021/694 of the European Parliament and of the Council of 29 April 2021 establishing the Digital Europe Programme and repealing Decision (EU) 2015/2240 (OJ L 166, 11.5.2021, p. 1, ELI: http://data.europa.eu/eli/reg/2021/694/oj).

(28) To facilitate access to technical expertise and ensure dissemination of knowledge across the Union, as well as support to diverse skills initiatives, the network of competence centres established under the Chips for Europe Initiative should continue ~~being~~**to operate and be** supported under the Chips for Europe Initiative 2.0**. The competence centres already selected by the Chips Joint Undertaking should remain part of that network. Member States should also have the possibility to designate additional candidate competence centres, which may join the network following their selection by the Chips Joint Undertaking**. To that end, the Chips Joint Undertaking established by Council Regulation (EU) 2021/2085[11] should establish the procedure for ~~continuing the support for~~**supporting the network and for the selection of additional** competence centres, including the **relevant** selection criteria, as well as further details on the implementation of the tasks and functions referred to in this Regulation. **As is the case for the existing competence centres, any additional**~~The~~ competence centres ~~forming~~**joining** the network should be selected by the Chips Joint Undertaking**. Competence centres forming the network** ~~and~~ should have substantial overall autonomy to lay down their organisation, composition, and working methods. However, their organisation, composition, and working methods should comply with and contribute to the objectives of this Regulation. **The network should contribute to the participation of stakeholders from all Member States and strengthen links with national semiconductor ecosystems and strategies.**

[11] Council Regulation (EU) 2021/2085 of 19 November 2021 establishing the Joint Undertakings under Horizon Europe and repealing Regulations (EC) No 219/2007, (EU) No 557/2014, (EU) No 558/2014, (EU) No 559/2014, (EU) No 560/2014, (EU) No 561/2014 and (EU) No 642/2014 (OJ L 427, 30.11.2021, p. 17, ELI: http://data.europa.eu/eli/reg/2021/2085/oj).

(29) Skills and education related work that is being carried out by the Union is fundamental to further flourishing the Union's semiconductor ecosystem **by addressing skills needs across the entire semiconductor value chain**. For that purpose, the STEM Education Strategic Plan[12] and its actions should be leveraged, and initiatives like the Pact for Skills[13], Skills Academies[14], joint European study programmes[15], the Skills Portability Initiative[16] and the European Universities Alliances[17] should contribute to the development of specific actions for the semiconductor sector. Similarly, in order to attract external talent to the Union, synergies with initiatives that facilitate international recruitment like the EU Talent Pool[18] should be explored. **Access to such infrastructure should contribute to the participation of stakeholders from all Member States. Access conditions should in particular ensure a genuine possibility for SMEs and research and knowledge-dissemination organisations to develop their own competences and technologies, with appropriate protection of confidentiality, intellectual property rights and agreed arrangements for further use of results.**

PUBLIC

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12 Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions 'A STEM Education Strategic Plan: skills for competitiveness and innovation'

13 https://pact-for-skills.ec.europa.eu/index_en

14 https://digital-strategy.ec.europa.eu/en/news/new-digital-skills-academies-support-eus-technological-sovereignty-competitiveness-and-preparedness

15 Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions 'a blueprint for a European degree'

16 https://ec.europa.eu/info/law/better-regulation/have-your-say/initiatives/15892-Fair-labour-mobility-package-Skills-portability-1-digitalised-cross-border-portability-of-qualifications-and-skills_en

17 https://education.ec.europa.eu/education-levels/higher-education/european-universities-initiative/map

18 Regulation (EU) 2026/1047 of the European Parliament and of the Council of 29 April 2026 establishing an EU Talent Pool

(30) Access to publicly funded infrastructure, such as pilot and testing facilities, and to the competence centres, should be open to a wide range of users and should be granted on a transparent and non-discriminatory basis and on market terms (or cost plus reasonable margin basis) for large undertakings, while SMEs and academic institutes may benefit from preferential access or reduced prices thereby facilitating broader participation in semiconductor innovation and supporting the development and diffusion of industrial capabilities across the Union. Moreover, the research and innovation activities under the Chips for Europe Initiative 2.0, including technology infrastructures, should also be to the benefit of the defence sector, without prejudice to further activities for the development of defence products and technologies that may take place under Regulation (EU) 2025/2643.

(31) The success of the Chips for Europe Initiative 2.0 can only be built on a collective effort of Member States and the Union to support the significant capital costs, to widen the availability of resources for virtual design, testing and piloting, and the diffusion of knowledge, skills and competences. Where appropriate, in view of the specificities of the actions concerned, the objectives of the Chips for Europe Initiative 2.0, in particular the Chips Fund activities, should also be supported through a blending facility under the InvestEU Fund. Support from the Chips for Europe Initiative 2.0 should be used to address, in a proportionate and cost-effective manner, market failures or sub-optimal investment situations as a consequence of high capital intensity, high risk, and complex landscape of the semiconductor ecosystem and actions should not duplicate or crowd out private financing or distort competition in the internal market. Actions should have a clear added value throughout the Union.

PUBLIC

(32) Moreover, the Chips for Europe Initiative 2.0 should continue building upon the strong knowledge base and enhance synergies with actions currently supported by the Union and Member States through programmes and actions in research and innovation in semiconductors and in developments of part of the value chain, in particular Horizon Europe and the Digital Europe Programme with the aim to reinforce the Union as global player in ~~semiconductor~~**chip** technology and its applications, with a growing global share in manufacturing, in accordance with Commission communication entitled '2030 Digital Compass: the European way for the Digital Decade'[19]. Furthermore, private investments are expected to be mobilised to complement the funding of the Chips for Europe Initiative 2.0 contributing to achieving its objectives. Complementing those activities, the Chips for Europe Initiative 2.0 would closely collaborate with other relevant stakeholders, including with the Industrial Alliance for Semiconductors.

PUBLIC

[19] Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, 2030 Digital Compass: the European way for the Digital Decade, COM(2021) 118 final, 9 March 2021.

(33) Research and development (R&D) within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Chips for Europe Initiative 2.0, it is necessary to adopt an approach to ensure that the access to and use of commercially sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Chips for Europe Initiative 2.0, are protected. To ensure that protection, any actions supported by the Chips for Europe Initiative 2.0 and funded by Horizon Europe and the Digital Europe Programme, as well as their **potential** successors under a subsequent Multiannual Financial Framework, should follow the relevant provisions of those programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security, exploitation and dissemination, transfer and licensing, and access rights. It is possible to set specific provisions when implementing those programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of commercially sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2004/48/EC and (EU) 2016/943 and[20] of the European Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council.

[20] Directive (EU) 2016/943 of the European Parliament and of the Council of 8 June 2016 on the protection of undisclosed know-how and business information (trade secrets) against their unlawful acquisition, use and disclosure (OJ L 157, 15.6.2016, p. 1, ELI: http://data.europa.eu/eli/dir/2016/943/oj).

(34) In order to strengthen the uptake of ~~semiconductors~~**chips** designed in the Union, manufactured in the Union, or both, across industrial value chains, it is necessary to promote closer linkages between semiconductor supply and downstream industrial demand, while remaining consistent with the Union's international obligations and competition rules. In particular, enhanced coordination between ~~semiconductor~~**chip** technology providers and users should facilitate the identification of aggregate demand, the development of common technical requirements, and the development of solutions tailored to Union industrial needs. Such coordination is especially relevant in key sectors such as cloud computing, automotive, aeronautical, telecommunications, defence and robotics, which are characterised by high-performance, security, reliability, and energy-efficiency requirements, and where ~~semiconductors~~**chips** constitute a critical enabling technology for innovation, digital transformation, and strategic autonomy. In those sectors, early engagement of users in the design and development phase can significantly reduce time-to-market, improve system integration, and ensure that semiconductor solutions are fit for purpose and aligned with evolving industrial standards and operational constraints. To that end, the Commission should, in cooperation with Member States and relevant stakeholders, put in place the necessary conditions for the Alliance for Semiconductor to facilitate industrial matchmaking, co-design activities and collaborative initiatives, ~~including~~**, in particular** through ~~a~~**the** demand forum **and demand accelerators. While the demand forum should facilitate exchanges between industrial users and chip technology providers and increase the visibility of available and emerging chip technologies, demand accelerators should stimulate the uptake of chips designed or manufactured within the Union by facilitating cooperation on industrial requirements, common technical roadmaps, co-design activities and collaborative projects. Together, those instruments should contribute**~~, with a view~~ to bridging the gap between supply and demand, fostering innovation ecosystems and accelerating the deployment of semiconductor-based solutions within the Union, in compliance with Union competition rules and in a manner consistent with the Union's international obligations. **Such activities should, where relevant, involve stakeholders from across the semiconductor value chain, including research and knowledge-dissemination organisations, competence centres and SMEs. For chips**~~For semiconductors~~ used in defence and space sectors, which are highly specialised and must operate reliably in extreme and hostile environments, the Commission should ~~continue to~~ coordinate the activities within the EU

Observatory of Critical Technologies for space and defence **with the activities within the relevant demand accelerators**.

(35) In **addition to the work undertaken by the relevant demand accelerator, for** the space and defence sector, activities aimed at identifying gaps, vulnerabilities and needs will continue ~~within~~**with** the already established EU Observatory of Critical Technologies (OCT). Specific EU technology roadmaps for space and defence, including semiconductors, responding to the OCT and covering research, innovation and industrialisation, will inform the EU work programme for space and defence development activities **and the work of the relevant demand accelerators**.

PUBLIC

(36) The demand forum should allow potential ~~offtakers of semiconductor~~**industrial users of chip** technologies to express their needs and expected specifications from an aggregated or industry-wide perspective, while enabling European semiconductor technology initiatives and strategic projects**, as well as integrated production facilities and open EU foundries recognised under Regulation (EU) 2023/1781,** to present their technological capabilities and proposed solutions. **The** demand ~~accelerator measures~~**forum should thus provide an interface between the Union's semiconductor ecosystem and downstream industrial users, increasing the visibility of available and emerging chip technologies and facilitating contacts and potential partnerships between suppliers and users. The implementation of the demand forum should be entrusted to the Industrial Alliance for Semiconductors. Building on its broad representation of actors across the semiconductor value chain and downstream industries, the Industrial Alliance for Semiconductors** should facilitate ~~collaborative platforms, pilot projects and design partnerships, enabling the early validation and deployment of innovative~~**the participation of relevant stakeholders and provide an industry-led environment for such exchanges. The European** Semiconductor ~~solutions within the Union. They can also contribute to growth of innovative ecosystems and facilitate the emergence of lead markets in key sectors, thereby enhancing the Union's industrial competitiveness and technological sovereignty. All~~**Board should be kept regularly updated on the** activities ~~carried out under~~**of the demand forum. In order to ensure that the needs of the entire semiconductor ecosystem are adequately reflected, particular attention should be paid to the effective participation and representation of SMEs, startups and scale-ups in** the demand forum and **related** demand accelerator measures~~ should be implemented in full compliance with Union competition law and other relevant provisions of Union law, ensuring that cooperation between undertakings does not lead to distortions of competition or the exchange of commercially sensitive information.~~**.**

PUBLIC

(36a) **Demand accelerator measures should build on such exchanges and stimulate the uptake of chips designed or manufactured within the Union, in particular in key markets. They should be implemented by the Industrial Alliance for Semiconductors through thematic working groups, as appropriate, which should provide a practical framework for cooperation between semiconductor actors and relevant downstream industrial sectors. In cooperation with the Commission, Member States and relevant industrial stakeholders, including start-ups, scale-ups, SMEs and small mid-caps, those working groups should facilitate discussions between potential users, in particular off-takers, on future requirements and technological specifications, enable the development of common technical roadmaps and support co-design between chip designers, chip manufacturers and downstream industrial users, including system integrators and equipment manufacturers, as well as facilitate collaborative platforms, pilot projects and design partnerships, enabling the early involvement of industrial users in the design, validation and deployment of innovative semiconductor solutions within the Union. Member States should endeavour to promote the participation of their industrial stakeholders in those activities.**

(36b) **Through this industry-led cooperation, the demand accelerators should help chip technologies developed and manufactured in the Union to respond more closely to the present and future requirements of downstream industries and enable users to become involved earlier in their development. They could also contribute to growth of innovative ecosystems and facilitate the emergence of lead markets in key sectors, thereby enhancing the Union's industrial competitiveness and technological sovereignty. All activities carried out under the demand forum and demand accelerator measures should be implemented in full compliance with Union competition law and other relevant Union law, ensuring that cooperation between undertakings does not lead to distortions of competition or the exchange of commercially sensitive information.**

PUBLIC

(37) In order to foster the widespread deployment of systems integrating ~~advanced semiconductor~~**innovative chip** technologies within the Union, it is necessary to **bridge the gap between semiconductor innovation and its market uptake by users. To that end, the Chips Joint Undertaking should** support ~~targeted~~**innovation procurement and the integration, qualification and first deployment of innovative chip technologies across the semiconductor value chain, including technologies developed within the Chips for Europe 2.0 initiative. It should also facilitate access to the technical expertise, infrastructure and support services necessary for their integration, testing, validation and qualification, including, where appropriate, by supporting** actions that ~~enhance~~**coordinate and provide such expertise and services to beneficiaries. Support could include financial support for activities necessary for the adoption of procured innovative chip technologies in users' systems, such as redesign, integration, testing, validation and qualification, including, where necessary, through financial support provided to third parties. Such actions should thereby reduce the technical and financial barriers associated with the first adoption of innovative chip technologies and contribute to creating early demand for such technologies.** Cooperation **between contracting authorities or contracting entities from different Member States should also be facilitated, where relevant and on a voluntary basis, including through buyer groups and**~~and innovation. In particular, facilitating the formation of~~ cross-border joint procurement arrangements~~ between contracting authorities or entities can~~**. Such cooperation could** help aggregate demand, reduce market fragmentation, and ~~enable more efficient~~**facilitate** investment in ~~complex and costly semiconductor-based systems. At the same time, supporting the integration and deployment of~~ innovative ~~semiconductor~~**chip** technologies ~~is essential to accelerate their uptake in key sectors, including digital infrastructure, artificial intelligence, and industrial applications, thereby strengthening the Union's technological capacity and competitiveness. To ensure the effective implementation of such actions, the Commission~~**and systems integrating such technologies. Support provided under this Regulation** should ~~provide technical and legal guidance to~~**not affect the responsibility of** contracting authorities~~. This guidance should support~~**,** contracting ~~authorities in using security of supply, cybersecurity, resilience, energy efficiency, lifecycle performance, supply-chain transparency and Union added-value criteria when procuring systems integrating innovative semiconductor design and solutions, in compliance~~**entities or purchasing entities for the preparation and conduct of procurement procedures and the award of contracts in accordance** with

applicable ~~Union law and~~ international**, Union and national law. Moreover, the Chips Joint Undertaking's support** ~~obligations. In particular, it~~ should ~~promote pre-commercial~~**not establish or modify rules governing public** procurement, ~~innovation partnerships and joint~~**but should facilitate the use of the possibilities available under the applicable** procurement ~~of procedures capable of creating early demand for trusted semiconductor technologies developed, produced or both, in the~~**framework, including any relevant future rules applicable at the time the procurement procedure is conducted. When assessing** Union **added value in innovation procurement, account should be taken of demonstrable technological contribution at the level of materials, devices, chips or integration technology, rather than merely the assembly of finished components or final system integration**.

(37a) In assessing the Union added value of a strategic project, account should be taken of where research, production and skills development take place, the retention of key know-how, intellectual property rights and assets, and the project's capacity to create lasting industrial capabilities after public support ends. Such elements may demonstrate the project's contribution to strengthening technological sovereignty, competitiveness and to ensuring that the benefits of public support increase the indispensability, prosperity and resilience of the Union.

PUBLIC

(38) In light of their importance for ensuring the security of supply and enabling a resilient semiconductor ecosystem, European semiconductor technology initiatives and strategic projects should be considered to be in the public interest. Ensuring the security of supply of ~~semiconductors~~**chips** is also important for digitalisation, which enables the green transition of many other sectors**. By reducing strategic dependencies, addressing vulnerabilities in semiconductor supply chains and strengthening critical capacities within the Union, strategic projects should contribute to increasing the economic security of the Union**. To attract investments to the Union's semiconductor sector and contribute towards security of supply of ~~semiconductors~~**chips** and resilience of the Union's semiconductor ecosystem, Member States may apply support measures, including incentives, and provide for administrative support in national permit-granting procedures for European semiconductor technology initiatives. In the Multiannual Financial Framework 2028-2034, National and Regional Partnership Plans may constitute part of the support, subject to the provisions of those plans. The possibility of support by Member States should be without prejudice to the competence of the Commission in the field of State aid under Articles 107 and 108 TFEU, where relevant. To ensure the correct and efficient application of the State aid rules, in its communication 'A Chips Act for Europe'[21], the Commission has already recognised the need for a case-by-case assessment regarding State aid granted to semiconductor production facilities with a view to safeguarding the Union's security of supply and supply-chain resilience while generating significant positive impacts on the wider economy. Furthermore, the procedures for the recognition as European semiconductor technology initiatives and for the authorisation of State aid, where applicable, should be conducted in parallel in order to accelerate the decision-making process. Member States should support the establishment of European semiconductor technology initiatives in accordance with Union law. When providing support measures for European semiconductor technology initiatives, Member States should consider setting non-discriminatory requirements related to intellectual property protection and security, including cyber-security, and confidentiality and could recommend mitigation measures to address specific risks related to the interference, forced technology transfers, and IP theft by entities from third countries. **Such support should respect the administrative**

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[21] Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, A Chips Act for Europe, COM(2022) 45 final, 8 February 2022.

structures and competences of the Member States and should not require the establishment of parallel national procedures or authorities.

(38a) In order to ensure continuity, consistency and administrative efficiency in the application of this Regulation, the procedure for submitting and assessing applications for the status of European semiconductor technology initiative should follow the same procedural approach as that established for applications for the status of integrated production facility and open EU foundry under Regulation (EU) 2023/1781. The Communication from the Commission of 20 August 2024 on the Guidance on the application for an undertaking to obtain the status of integrated production facility and open EU foundry pursuant to Article 15 of the Chips Act Regulation (EU) 2023/1781 should continue to apply, mutatis mutandis, to the application procedure for the status of European semiconductor technology initiative, to the extent that it is compatible with this Regulation and until such guidance is replaced or updated. This should ensure continuity in the information to be provided by applicants, the format of applications and the assessment of applications, while taking account of the specific requirements applicable to European semiconductor technology initiatives under this Regulation.

(39) In order to encourage the establishment of the necessary related design capabilities, Member States may provide support for such activities in accordance with State aid rules, including under framework for State aid for research and development and innovation[22] or Commission Regulation (EU) No 651/2014[23].

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[22] Communication from the Commission Framework for State aid for research and development and innovation (C/2022/7388) (OJ C 414, 28.10.2022, p. 1).

[23] Commission Regulation (EU) No 651/2014 of 17 June 2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty (OJ L 187, 26.6.2014, p. 1, ELI: http://data.europa.eu/eli/reg/2014/651/oj).

(40) In order to encourage the establishment of the necessary manufacturing and related design capabilities, and thereby ensure the security of supply and strengthen the resilience of the Union's semiconductor ecosystem, public support may be appropriate, provided that this does not lead to distortions in the internal market. In that respect, it is necessary to harmonise certain conditions for operators to carry out specific projects at Union level that contribute to achieving the objectives of this Regulation and establish a framework for recognising European semiconductor technology initiatives.

(41) European semiconductor technology initiatives should provide capabilities that are 'first-of-a-kind' in the Union and contribute to the **competitiveness,** indispensability, resilience, prosperity~~, competitiveness~~ and security of supply of the Union's semiconductor ecosystem. The qualifying factor for being a 'first-of-a-kind' initiative is to bring an innovative element to the internal market regarding the manufacturing processes or the final product, which could be based on new or existing technology nodes, including mature and cutting-edge ones. An initiative providing an innovation with regard to the manufacturing process or final product which is similar to an innovation which already exists or is already planned in the Union may still be recognised as first-of-a-kind if it can be demonstrated that the initiative is necessary to ensure the Union's resilience and security of supply by reducing excessive strategic dependencies on imports from third countries. Any such initiative should be assessed based on its own merits, taking into account, for instance, relevant market analysis, the degree of concentration of the dependencies and the risk of creating a situation of overcapacity. **Where relevant, the assessment should also recognise the strategic importance of specialised and niche capabilities, including where these are developed by smaller ecosystems or Member States without large-scale manufacturing capacity.**

(42) Relevant innovation elements in first-of-a-kind initiatives could relate to the technology node or substrate material, or approaches that lead to improvements in computing power or other performance attributes, energy efficiency, level of security, safety or reliability, as well as integration of new functionalities, such as AI, memory capacity or other. Integration of different processes leading to efficiency gains**, advanced packaging technologies, testing methodologies, photonic integration** or packaging and assembly automation are also examples of innovation. With regard to environmental gains, innovation elements would include the reduction in a quantifiable way of the amount of energy, water or chemicals used, or improving recyclability.

(42a) **The semiconductor manufacturing equipment sector is characterised by highly specialised equipment, a high variety of equipment configurations and comparatively low production volumes, with equipment solutions often being realised through specialised engineering, integration, testing, validation and qualification processes, in close cooperation with users, to meet specific process, performance and manufacturing requirements. These steps may be closely linked to the introduction of innovative chip manufacturing processes or capabilities in the Union and thereby contribute to the indispensability, resilience and prosperity of the Union's semiconductor ecosystem. In this context, the notion of 'process for the production of equipment' in the definition of first-of-a-kind initiatives can include the engineering, integration, testing, validation and qualification activities that are directly linked and necessary for the production of equipment. Accordingly, where an initiative concerns such a new or substantially upgraded process for the production of equipment that is linked to and enables innovation with regard to the equipment manufacturing process or final product to the extent that this innovation is not yet sufficiently present or committed to be built within the Union to ensure the Union's resilience and security of supply, it should be considered as a first-of-a-kind initiative.**

(43) In order to ensure public investments in European semiconductor technology initiatives and strategic projects lead to an actual increase in security of supply and resilience of the Union, undertakings applying for recognition or support under this Regulation should demonstrate that they will articulate their supply chain in a way that reduces **critical** supply chain ~~dependence~~**dependencies** on non-domestic ~~undertakings~~**entities and promote the inclusion of Union entities across the semiconductor value chain**. Such information should include, where applicable to the initiative's activities, the origin of the essential ~~semiconductor~~**chip** manufacturing equipment and substrates and the extent to which procurement from third country undertakings is necessary due to technical performance considerations. In the case of front-end or back-end ~~semiconductor~~**chip** manufacturing, undertakings should also indicate the other relevant front-end or back-end manufacturing processes beforehand or afterwards linked to the investment taking place within and outside the Union.

(44) In order to facilitate ~~semiconductor~~**chip** manufacturing investments, public authorities should take into account the necessary enabling conditions for the sustainable operation of such facilities, including access to energy, water and other critical infrastructure resources. To support the long-term resilience and sustainability of the semiconductor ecosystem in the Union, appropriate consideration should be given to the expected resource needs and environmental impacts associated with such investments.

(45) Where a European semiconductor technology initiative offers production capacity to undertakings not related to the operator of the facility, it should establish, implement and maintain adequate and effective functional separation in order to prevent the exchange of confidential information between internal and external production. This should apply to any information obtained in the design and in the front-end or back-end manufacturing processes**, while ensuring that the implementation of such requirements remains proportionate and avoids unnecessary administrative burdens, taking into account the specific business model and technological characteristics of the initiative**.

PUBLIC

46) In order to qualify as a European semiconductor technology initiative, the establishment of the initiative by a domestic ~~undertaking~~**entity** should have a clear positive impact with spill-over effects beyond the undertaking or the Member State concerned on the Union's semiconductor value chain in the medium to long term with a view to strengthening resilience, competitiveness and innovation of the semiconductor ecosystem, including the growth of start-ups and SMEs, and contributing to the Union's twin green and digital transitions. Moreover, following the same reasoning, participation in the Business-to-Business Semiconductor Supply Chain Platform ('the Platform') should be obligatory for production facilities – such as front-end and back-end production facilities, but also other production facilities like for the production of ~~semiconductor~~**chip** manufacturing equipment, substrates or materials. This commitment serves the strengthening of the resilience, competitiveness and innovation of the semiconductor ecosystem's supply chains. Various activities of domestic ~~undertakings~~**entity** aiming to create positive spill-over effects may be considered for the purpose of qualifying as European semiconductor technology initiatives. Examples include giving access to manufacturing facilities against a market fee; giving process design kits to smaller design companies or to the virtual design platform; disseminating results from their R&D activities; engaging in research collaboration with European ~~universities and~~ research ~~institutes~~**and knowledge-dissemination organisations**; cooperating with national authorities or educational and vocational institutions to contribute to skills development; contributing to Union-wide research projects; or offering dedicated support opportunities for start-ups and SMEs. The impact on several Member States, including with regard to cohesion objectives, should be considered as one of the indicators of a clear positive impact of a European semiconductor technology initiative on the semiconductor value chain in the Union.

PUBLIC

(47) In order to ensure legal clarity and consistent application of this Regulation, it is necessary to clarify the conditions under which an undertaking may be recognised as a European semiconductor technology initiative. Experience with the implementation of the framework for integrated production facilities and open EU foundries under Regulation (EU) 2023/1781 has shown that uncertainties have arisen among undertakings and Member States as to whether the status of a semiconductor technology facility is conditional upon the receipt of public support. It should therefore be explicitly clarified that, while an application for such status should relate to a first-of-a-kind initiative, the granting of the status should not be dependent on the receipt of support measures or administrative assistance. Consequently, first-of-a-kind initiatives may obtain the status of a European semiconductor technology initiative irrespective of whether they benefit from public funding, provided that they comply with the relevant requirements set out in this Regulation.

(48) It is important that European semiconductor technology initiatives are not subject to extraterritorial application of public service obligations imposed by third countries that could undermine their ability to use or re-export the final product stemming from their infrastructure, software, services, facilities, assets, resources, IP or know-how needed to fulfil their obligations under this Regulation, in particular those related to security of supply.

(49) In light of the fast development of ~~semiconductor~~**chip** technologies and to strengthen the future industrial competitiveness of the Union, European semiconductor technology initiatives should invest in the Union in continued innovation with a view to achieving concrete advances in ~~semiconductor~~**chip** technology or preparing next-generation technologies. Such initiatives should be able to test and experiment new developments through preferential access to the pilot lines established under the Chips for Europe Initiative in Regulation (EU) 2023/1781 and the Chips for Europe Initiative 2.0 through fast-tracked applications. Any such preferential access should neither exclude nor prevent effective access on fair terms to the pilot lines by other interested undertakings, in particular start-ups and SMEs. Taking into account the importance of a qualified and skilled workforce to achieve the objectives of this Regulation, European semiconductor technology initiatives should support the Union talent pipeline by developing and deploying educational and skills training and by increasing the pool of qualified and skilled workforce.

(49a) **European semiconductor technology initiatives should support continued innovation across the semiconductor value chain and should not be limited to leading-edge or cutting-edge semiconductor technologies. Innovation and strategic importance could also concern mature or existing technology nodes where the initiative introduces innovative elements, strengthens the Union's competitiveness, resilience or security of supply, or addresses strategic dependencies in important semiconductor technologies or industrial applications. This approach is consistent with the recognition of first-of-a-kind initiatives based on new or existing technology nodes, including mature and cutting-edge technologies.**

(50) To allow for a uniform and transparent procedure to attain the status as a European semiconductor technology initiative, the decision to grant this status should be adopted by the Commission following the application by an individual undertaking or a consortium of several undertakings. The status should be open for both the installation of a new ~~semiconductor~~**chip** manufacturing initiative and the significant scale-up or innovative transformation of an existing ~~semiconductor~~**chip** manufacturing initiative. To account for the importance of a coordinated and cooperated implementation of the planned facility, where relevant, the Commission should take into account in its assessment the readiness of one or more Member States where the applicant intends to establish its initiatives to support the establishment of such initiatives. Furthermore, when assessing the viability of the business plan, the Commission could take into account the overall record of the applicant as well as the existence of appropriate measures to protect intellectual property and commercially sensitive information. **The assessment should be based on transparent, objective and technology-neutral criteria.**

PUBLIC

(50a) **The status of a European semiconductor technology initiative and the designation of a strategic project pursue complementary but distinct objectives and entail different requirements. The status of a European semiconductor technology initiative is a voluntary status granted to a project which qualifies as a first-of-a-kind initiative and is intended, in particular, to give visibility at Union level to European initiatives that contribute to the Union's semiconductor ecosystem and comply with the requirements laid down in this Regulation. The designation of a strategic project is intended to recognise projects of particular strategic importance to the Union which provide significant Union added value, have a clear cross-border dimension and contribute to strengthening the Union's technological sovereignty and leadership, as well as the competitiveness, indispensability, resilience and prosperity of the Union's semiconductor value chain. Strategic project status is not conditional on the project being first-of-a-kind, although the designation decision may confirm such status where the applicable conditions are met.**

(51) In light of the rights attached to recognition as a European semiconductor technology initiative, the Commission should monitor whether initiatives that have been granted that status continue to comply with the requirements set out in this Regulation. If this is no longer the case, the Commission should have the right to re-examine and, if necessary, repeal the status and, accordingly, the rights attached to that status. Any decision to repeal that status should be taken only after consulting the European Semiconductor Board and should be properly reasoned. Correspondingly, the undertaking operating a European semiconductor technology initiative should have the possibility to proactively request a review of the duration of the status or implementation plans where unforeseen external circumstances, such as serious disturbances with a direct economic impact on the recognised initiative, could have an impact on its ability to comply with the applicable criteria. **Where appropriate, the undertaking should have the possibility to propose corrective measures before the status is withdrawn.**

(52) In order to strengthen the Union's technological sovereignty, **competitiveness,** resilience, indispensability~~, competitiveness~~ and prosperity in the semiconductor sector, it is necessary to identify and support projects of strategic importance by domestic ~~undertakings~~**entities** across the semiconductor value chain. Strategic projects on semiconductors should be granted support from Union programmes, funds and financial instruments, in accordance with the objectives set out in the regulation establishing those funds and programmes and without prejudice to the next (2028-2034) multiannual financial framework. In particular, those strategic projects should be granted the competitiveness seal where they fulfil the conditions set out in Regulation (EU) 2026/XXX [on establishing the European Competitiveness Fund] (ECF') ([1]), as high-quality projects that contribute to the objective of the European Competitiveness Fund. Strategic projects should contribute to objectives of common Union interest and reinforce the Union's capacity to design, manufacture and integrate advanced ~~semiconductor~~**chip** technologies and demonstrate clear Union added value and a cross-border dimension, in particular through cooperation between Member States or through coordinated public support. They should contribute to strengthening the resilience and robustness of the Union's semiconductor ecosystem, including by addressing bottlenecks, reinforcing semiconductor supply chains and enhancing innovation and industrial deployment. The participation of innovative SMEs and ~~SMCs~~**small mid-caps** in strategic projects shall be encouraged. **Strategic importance should be assessed on the basis of the contribution to the Union semiconductor ecosystem and supply-chain resilience as a whole, rather than primarily on the scale of manufacturing capacity.**

PUBLIC

(53) Both strategic projects and European semiconductor technology initiatives should be able to focus not only on cutting-edge semiconductor nodes, but also on innovative existing and mature technology nodes where this is necessary to preserve and strengthen the Union's competitiveness, resilience and security of supply across strategically important ~~semiconductor~~**chip** technologies and industrial applications. In order to ensure that strategic projects effectively contribute to the Union's long-term competitiveness, such projects should support the development or deployment of critical capacities, technologies or capabilities within the Union. This should include, in particular, activities that reduce strategic dependencies and enhance the Union's technological leadership in key segments of the semiconductor value chain~~, including by enabling, advancing or securing critical technologies and capabilities within the Union.~~**. This should be without prejudice to existing bottom-up procedures.**

(53a) The strategic importance of a project should be assessed on the basis of the criteria laid down in this Regulation and not on the basis of its financial, operational or other size. A project may qualify as a strategic project irrespective of the amount of investment involved, its scale or the size of the entities participating in it, provided that it meets the requirements laid down in this Regulation.

(54) Where strategic projects are implemented across multiple sites, they should be carried out by a single consortium and function as an integrated entity, in order to ensure coherence, efficiency and effective coordination of activities.

(55) In light of the strategic nature of the semiconductor sector and its relevance for security, participation in strategic projects should be subject to appropriate conditions. In accordance with Article 136 of Regulation (EU, Euratom) 2024/2509 of the European Parliament and of the Council[24], it would be possible to restrict or exclude the participation of certain entities where this would be contrary to the Union's strategic assets, interests, autonomy or security. As a general rule, participation in strategic projects should be limited to legal entities established in the Union. However, by way of derogation and where duly justified, participation may be extended to entities established in third countries, provided that such participation complies with the applicable conditions and safeguards**, contributes clear added value to the project** and does not undermine the Union's strategic assets, interests, autonomy or security.

(56) To ensure flexibility and to reflect technological developments and evolving market needs, this Regulation should set out a list of indicative technological areas for strategic projects**. In identifying priority areas the Commission should take into account vulnerabilities and strategic capabilities across the entire value chain**. The power to amend that list should be delegated to the Commission in accordance with Article 290 TFEU in order to update those areas in light of technological change and market developments relevant to the semiconductor sector. In order to ensure a coherent and efficient identification and selection of strategic projects, the Commission, taking into account the opinion of the European Semiconductor Board, should identify priority areas and establish a list of topics of potential projects. The implementation of actions supporting such projects should be carried out, where appropriate, through the Chips Joint Undertaking, in accordance with its governing Regulation and work programmes. To strengthen the Union's sovereignty and ensure security of supply in leading-edge ~~semiconductors~~**chips**, it is appropriate to prioritise the establishment of an open foundry for advanced ~~semiconductor~~**chip** manufacturing capabilities within the Union, which should operate, where relevant, on the basis of open access for different users. That strategic project could be complemented by other strategic projects on for instance memory, design, and other ~~semiconductor~~**chip** technologies.

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[24] Regulation (EU, Euratom) 2024/2509 of the European Parliament and of the Council of 23 September 2024 on the financial rules applicable to the general budget of the Union (OJ L, 2024/2509, 26.09.2024, ELI: http://data.europa.eu/eli/reg/2024/2509/oj).

(57) **The implementation of strategic projects should commence only once the relevant legal and financial framework under the subsequent Multiannual Financial Framework is in place. Without prejudging the co-legislators' prerogatives, such implementation should be carried out, where applicable, by a successor entity or initiative to the Chips Joint Undertaking established under Council Regulation (EU) 2021/2085 or by another structure entrusted with the relevant implementation tasks. Until then,** the Chips Joint Undertaking should ~~implement actions supporting strategic projects through its work programme, including through calls for proposals in accordance with its applicable rules~~**continue to exercise the tasks entrusted to it under its existing legal framework**. Proposals should be evaluated in accordance with the procedures and criteria ~~set out in the governing framework of the Chips Joint Undertaking~~**applicable to the entity, initiative or other structure entrusted with those implementation tasks**. In order to ensure efficiency and avoid duplication of assessments, the Commission should rely on the outcome of ~~the~~ **that** evaluation ~~carried out by the Chips Joint Undertaking~~ when designating strategic projects. Projects selected for funding ~~by the Chips Joint Undertaking~~**following such evaluation** and complying with the criteria laid down in this Regulation should be eligible for designation as strategic projects~~.~~

PUBLIC

(58) The designation of a project as a strategic project should be without prejudice to the outcome of funding decisions taken under the Chips Joint Undertaking. Projects not selected for Union funding should nevertheless be able to obtain the status of strategic project, subject to the consent of the applicant, in order to benefit from the rights and obligations attached to that status under this Regulation. Rights include strategic projects' inclusion in the demand forum, the possible receipt of public support and administrative support and the receipt of status of overriding public interest and possibly status of highest national significance relevant to permit-granting procedures, and obligations also applicable to European semiconductor technology initiatives, such as participation in the Business-to-Business Semiconductor Supply Chain Platform and the obligation to accept priority-rated orders. Strategic projects should benefit from the same rights and be subject to the same obligations as European semiconductor technology initiatives, where they comply with the relevant requirements, in order to ensure a coherent regulatory framework and to maximise their contribution to the Union's objectives in the semiconductor sector. Where relevant, such designation should also confirm their status as first-of-a-kind initiatives and define the duration of that status based on the expected lifetime of the project.

(59) In order to ensure that strategic projects continue to fulfil the criteria laid down in this Regulation, the Commission should be able to withdraw the designation of a project where those criteria are no longer met or where the designation was based on incorrect information. Before adopting such a decision, the Commission should ensure that the ~~undertakings~~**entities** concerned are given the opportunity to be heard, in accordance with the principle of good administration, and should take into account the opinion of the European Semiconductor Board**. Where appropriate, entities should be given the possibility to propose corrective measures before the designation is withdrawn**. Where the designation of a strategic project is withdrawn, that project should lose all rights and obligations associated with that status under this Regulation. However, such projects should remain subject, for a limited period, to specific obligations linked to security of supply, where provided for in this Regulation.

PUBLIC

(60) In order to guarantee simple and rapid permit-granting, Member States should ensure that permit-granting procedures for European semiconductor technology initiatives and strategic projects are organised through a ~~single~~ procedure based on a single application. Additionally, Member States should designate ~~a one-stop shop acting as~~ a single point of contact for the project, in order to facilitate and coordinate the processing of applications in an efficient, transparent and timely manner**, while respecting national administrative structures and competences**.

(61) It is necessary that European semiconductor technology initiatives and strategic projects are established as quickly as possible, while keeping the administrative burden to a minimum. For that reason, Member States should process applications related to the planning, construction and operation of such facilities in the most rapid manner possible. In order to further accelerate the deployment of European semiconductor technology initiatives and strategic projects, clear ~~and binding~~ time limits should be established for permit-granting procedures. In particular, the overall duration of such procedures should not exceed ~~the defined period of~~ 12 months ~~from the submission of a complete~~**after the date of acknowledgement by the single point of contact of the completeness of the** application, without prejudice to **any** shorter time limits set by Member States.

(61a) In exceptional and duly justified cases related to the nature, complexity, location or size of a European semiconductor technology initiative or strategic project, Member States should be able to extend the applicable time limit for the permit-granting procedure for a maximum of 6 months. Such exceptional circumstances could include unforeseen circumstances arising in the course of the procedure which could not reasonably have been anticipated when the application was submitted and which materially affect the timely completion of the procedure. Any such extension should be limited to what is strictly necessary and should be decided on a case-by-case basis before the expiry of the applicable time limit. Where the project concerned is a strategic project and has been selected to receive Union funding, the Commission should be informed without undue delay of the extension and of the reasons justifying it, so as to enable it to take those circumstances into account in the implementation and monitoring of the relevant Union support.

PUBLIC

(61b) **The fast-tracking of procedures under this Regulation should be achieved without prejudice to the requirements laid down in Union and national law concerning environmental protection, public participation, access to justice and the quality and completeness of administrative assessments. Acceleration should be pursued in particular through improved coordination between competent authorities, the digitalisation of procedures, early identification and scoping of the documentation required for the assessment of applications, and the avoidance of unnecessary duplication of assessments, studies, permits or authorisations. Such acceleration should not affect the substantive requirements applicable to the assessment or the rights of affected individuals and communities.**

(62) Given the potential cross-border nature of European semiconductor technology initiatives and strategic projects, Member States should make best efforts to effectively cooperate and coordinate at the level of relevant authorities, including between designated ~~one-stop shops~~**single points of contact**, in order to facilitate coherent and timely decision-making processes.

(63) Digitalisation of permit-granting procedures is essential to enhance transparency, efficiency and legal certainty. Member States should therefore establish single access portals at national level enabling applicants to submit and manage their applications in a fully digital environment. The use of interoperable digital solutions, including European Business Wallets **and existing structures established by Member States or Union law**, should facilitate secure data exchange, re-use of existing information and seamless interaction between applicants and competent authorities, while ensuring a high level of cybersecurity and data integrity. To improve transparency and predictability for applicants, the single access portal should provide up-to-date information on the status of applications, applicable procedures and deadlines, as well as notifications of decisions taken by the competent authorities.

(63a) **In order to facilitate access to financing for European semiconductor technology initiatives and strategic projects, it is appropriate to provide for a mechanism enabling the financing difficulties faced by such initiatives or projects to be identified and addressed in a coordinated manner. Difficulties in accessing financing could, in particular, arise where an initiative or project faces a material financing gap despite reasonable efforts to secure financing from available public or private sources, where the capital intensity, risk profile, scale or cross-border nature of the initiative or project limits the availability or suitability of financing, or where the available financing instruments do not adequately correspond to the financing needs or stage of development of the initiative or project. A Member State should be able to request advice from the European Semiconductor Board on behalf of a European semiconductor technology initiative or strategic project, including by means of a written request, setting out, where appropriate, the relevant financing needs and information on financing already secured. In providing such advice, the European Semiconductor Board should take into account existing public and private financing and consider relevant Union, national, regional and other sources of financing, including financial institutions and national promotional banks and institutions. Given that the European Semiconductor Board has a broader chip policy role, it should be possible, where appropriate, to invite or consult technical experts from the Member States with expertise in investment, financing or financial instruments in order to support the Board's consideration of such financing matters.**

PUBLIC

(64) Similarly, in order to support investment decisions and reduce information asymmetries, Member States should make relevant information on permit-granting procedures, financing opportunities, business support services and applicable regulatory requirements available online in ~~a centralised and~~**an** easily accessible manner. They should also ensure appropriate use of existing studies, permits and authorisations related to the planning, construction and operation of European semiconductor technology initiatives and strategic projects, where compatible with Union and national law, in order to avoid duplication of administrative procedures and reduce delays. Given the strategic importance and time sensitivity of European semiconductor technology initiatives and strategic projects, **it is important that** Member States ~~should~~ ensure that administrative and judicial proceedings related to permit-granting are treated as urgent, where and to the extent provided for under national law, while fully respecting the rights of defence and the rights of affected individuals and communities.

(64a) In view of the strategic importance and time sensitivity of European semiconductor technology initiatives and strategic projects, Member States should, in accordance with their applicable legal frameworks, seek to ensure that administrative and judicial proceedings related to permit-granting are handled as efficiently and, where provided for under national law, as a matter of priority or urgency. Such arrangements should fully respect the rights of defence and the rights of affected individuals and communities and the requirements of effective judicial protection under Union law. This Regulation should not be understood as requiring Member States to exclude or limit the suspensive effect of judicial proceedings or remedies where such effect is provided for under Union or national law, nor as harmonising national rules of judicial procedure. The application of any time limit under Union law should therefore remain without prejudice to the applicable national procedural rules governing judicial proceedings and remedies.

PUBLIC

(65) Regulation (EU) [202X/XX] of […][25] establishes a common acceleration framework for environmental assessments in order to boost the Union's roll out of key technologies, reduce dependencies and strengthen competitiveness. Procedures linked to environmental assessments should be accelerated and streamlined for plans, programmes and projects across all sectors of the economy while maintaining high levels of protection of human health and of the environment. Some sectors may, however, require yet faster environmental assessments. Therefore, and in order to safeguard the coherence of the legal framework of environmental assessments, while allowing for the additional needs for acceleration in certain strategic sectors, Regulation (EU) [202X/XX] establishes a dedicated toolbox that should therefore be used in the context of this Regulation. Given the essential role of ~~semiconductor~~**chip** technologies in ensuring the achievement of the Union's climate objectives by the introduction of novel, more sustainable technologies, production processes, the integration of ~~semiconductors~~**chips** in net-zero technologies, and their contribution to the Union's resilience and economic security, European semiconductor technology initiatives and strategic projects in the meaning of this Regulation should also be considered strategic projects within the meaning of Regulation (EU) [202X/XX] and therefore benefit from the dedicated toolbox established under that Regulation**, while ensuring full compliance with applicable Union environmental legislation and respecting the competences of Member States**.

[25] Proposal for a Regulation of the European Parliament and of the Council on speeding-up environmentalassessments (COM/2025/984 final, 10.12.2025).

(66) In the semiconductor sector, undertakings thrive in specialised local districts that can attract investment, foster innovation, and build resilient industrial ecosystems. Regions and regional industrial clusters are instrumental in developing and facilitating the establishment of such ecosystems. A European Semiconductor Region of Excellence label should be established with the objective of identifying, recognising and fostering regions in the Union that demonstrate a long-term, coordinated strategy to host, attract and expand semiconductor-related investments and semiconductor value chains. International investors should be able to find in a European Semiconductor Region of Excellence the ideal environment to develop semiconductor-related business. Such **a** label should be awarded by the Commission following applications by regional authorities, **which should be based on a long-term, coordinated strategy to host, attract and expand semiconductor-related investments and semiconductor value chains**~~on the basis of coherence and credibility~~ of a Semiconductor Region Investment Plan and the level of commitment by the relevant authorities, and the application should be endorsed by the relevant Member State in order to ensure political coordination between different levels of government.

(67) Applying regions should develop a Semiconductor Region Investment Plan. Measures proposed in that plan should address ~~in particular~~**, where relevant,** framework conditions to strengthen ~~semiconductor~~**chip** manufacturing, R&D collaboration, skills development, or sustainable infrastructure and signal their readiness to host semiconductor investments.

(68) On receiving the label, a region should gain access to opportunities, including stronger partnerships with industry and research institutions, and increased attractiveness to international investors seeking reliable, high-potential locations. Recognised regions should be able to join a Network of European Semiconductor Regions of Excellence, enabling them to share knowledge, forge alliances, and amplify their impact across the Union, while international recognition of their strategies would reinforce their reputation as prime destinations for semiconductor innovation and investment. **Where relevant, the Network should promote cooperation between regions specialising in different segments of the semiconductor value chain and facilitate the exchange of best practices.**

PUBLIC

(68a) **The European Semiconductor Region of Excellence label should help regions increase their visibility and attractiveness and facilitate access to relevant funding opportunities, including by allowing the label to be taken into account, where appropriate, in the assessment and selection under Union funding programmes, including relevant regional development funds. The award of the label should not, however, confer an entitlement to Union or national funding, nor should it constitute a funding decision as such. Where a Member State has adopted a national semiconductor strategy, roadmap or investment plan, relevant elements of such a national measure may, where appropriate, be reflected or taken into account in the Semiconductor Region Investment Plan, while the two plans should remain distinct instruments with their respective scope and responsibilities. The label should support not only regions with established chip ecosystems but also regions seeking to develop or expand emerging ecosystems. Accordingly, the assessment should focus on the coherence and credibility of the region's strategic vision, investment plan and commitment by the relevant authorities, and should not require the existence of a complete or fully developed chip ecosystem.**

(68b) **In order to strengthen cooperation between regions that have been awarded the European Semiconductor Region of Excellence label, a Network of European Semiconductor Regions of Excellence (the 'Network') should be established. The Network should promote cooperation and the exchange of information and best practices across all relevant segments of the semiconductor value chain and should build on and complement existing regional cooperation initiatives, including the European Semiconductor Regions Alliance (ESRA), while avoiding unnecessary duplication of structures and activities. The Network should be open to all regions interested in participating in its activities. Regions should therefore be able to apply to participate in the Network, subject to the conditions laid down in this Regulation. Following a Commission Decision awarding the European Semiconductor Region of Excellence label, the Network should be informed of the new membership without undue delay, so that the newly participating region can be involved in the activities of the Network from an early stage.**

PUBLIC

(69) ~~Semiconductors~~**Chips** are essential components embedded in infrastructures, equipment and systems used by critical entities, including those covered by Directive (EU) 2022/2555 of the European Parliament and of the Council[26]. The functioning, security and continuity of such critical entities depend increasingly on the availability, integrity and trustworthiness of ~~semiconductor~~**chip** components and of their suppliers. In order to reduce the Union's exposure to supply chain shocks and dependencies on a limited number of third-country suppliers, it is necessary to strengthen transparency and resilience in the sourcing of ~~semiconductors~~**chips** used in public procurement for critical infrastructures and services. Public procurement governed by Directives 2014/23/EU[27], 2014/24/EU[28], 2014/25/EU[29], of the European Parliament and of the Council represents a significant share of Union demand and can play a strategic role in promoting reliable and resilient semiconductor supply chains. Contracting authorities or contracting entities procuring critical infrastructure should integrate security of supply considerations throughout the procurement process~~,~~ and should also consider how the ~~semiconductors~~**chips** incorporated into the procured equipment or systems add value to the Union semiconductor supply chain resilience with their design and manufacturing steps. Such considerations are without prejudice to the Union cybersecurity legislation.

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26 Directive (EU) 2022/2555 of the European Parliament and of the Council of 14 December 2022 on measures for a high common level of cybersecurity across the Union, amending Regulation (EU) No 910/2014 and Directive (EU) 2018/1972, and repealing Directive (EU) 2016/1148 (NIS 2 Directive) (OJ L 333, 27.12.2022, p. 80, ELI: http://data.europa.eu/eli/dir/2022/2555/oj).

27 Directive 2014/23/EU of the European Parliament and of the Council of 26 February 2014 on the award of concession contracts (OJ L 94, 28.3.2014, p. 1, ELI: http://data.europa.eu/eli/dir/2014/23/oj).

28 Directive 2014/24/EU of the European Parliament and of the Council of 26 February 2014 on public procurement and repealing Directive 2004/18/EC (OJ L 94, 28.3.2014, p. 65, ELI: http://data.europa.eu/eli/dir/2014/24/oj).

29 Directive 2014/25/EU of the European Parliament and of the Council of 26 February 2014 on procurement by entities operating in the water, energy, transport and postal services sectors and repealing Directive 2004/17/EC (OJ L 94, 28.3.2014, p. 243, ELI: http://data.europa.eu/eli/dir/2014/25/oj).

(70) Encouraging contracting authorities and contracting entities to require economic operators to provide a security of supply declaration concerning the sourcing of ~~semiconductors~~**chips** would enhance transparency across supply chains and enables informed decision-making in procurement procedures, without imposing disproportionate administrative burdens and leaving discretion to contracting authorities and contracting entities as to whether to request such declaration in all procurement procedures. Such declaration should, where required, contain key elements enabling an assessment of supply chain robustness, including the identification of undertakings involved, the diversity of suppliers, added value to the Union's semiconductor supply chain resilience, strategies to increase resilience such as through dual sourcing from domestic ~~undertakings~~**entities**, and vulnerability assessments to potential disruptions, as well as, where applicable, relevant risk assessments carried out pursuant to this Regulation. To ensure that considerations of resilience, security and European supply chain added value are effectively integrated into procurement decisions, contracting authorities and contracting entities may specify in the procurement documents requirements relating to security of supply relating to the sourcing of ~~semiconductors~~**chips** incorporated into the infrastructures, equipment or systems covered by the public procurement contract. To that end, they may include technical specifications, selection criteria, award criteria or contract performance clauses.

The public procurement framework established by Directives 2014/24/EU, 2014/25/EU and 2009/81/EC contains provisions enabling contracting authorities to exclude economic operators that have been guilty of serious misrepresentation, have withheld relevant information, or have supplied false or misleading information in the context of participation in a procurement procedure. Those provisions remain applicable to procurement procedures carried out by national contracting authorities covered by this Regulation.

PUBLIC

(71) In this context, given that free trade agreements, custom unions, the WTO Agreement on Government Procurement[30] contain commitments on access to public procurement, undertakings from third countries which have concluded such international agreements with the Union guaranteeing such access should be deemed to fall under the definition of domestic ~~undertakings~~**entities**. Furthermore, these international agreements, as well as strategic partnerships on semiconductors, reflect a mutual commitment between the Union and its partners to secure international semiconductor supply chains, which is why undertakings from these Union partners are granted equivalence to domestic ~~undertakings~~**entities**. **Requirements applied in procurement should be without prejudice to the Union's commitments concerning equal treatment in access to public procurement markets and rules for determining the origin of goods.**

(71a) In order to allow contracting authorities and contracting entities, as well as economic operators, sufficient time to adapt their procurement procedures, procurement documents and internal processes to the requirements concerning security of supply declarations, the application of the provisions on public procurement laid down in this Regualtion should apply only to procurement procedures launched on or after the date falling one year after the entry into force of this Regulation. This transitional period should be without prejudice to preparatory measures that contracting authorities, contracting entities and economic operators may undertake before that date.

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30 Protocol Amending the Agreement on Government Procurement (OJ L 68, 7.3.2014, p. 2, ELI: http://data.europa.eu/eli/prot/2014/115/oj), which entered into force on 6 April 2014 (OJ L 89, 25.3.2014, p. 5).

(72) For the purposes of this Regulation, the assessment for whether an ~~undertaking~~**entity** is domestic or equivalent, or not, should look into the ownership structure and the control of such ~~undertaking~~**entity**. For assessing control, undertakings should be considered to be controlled by a third country or by a third-country legal entity, where that third country or legal entity is able to exercise decisive influence over its strategic decisions, whether directly or indirectly, including in particular, by having the right or exercising the power to appoint or remove a majority of the members of the administrative, management or supervisory body of the undertaking being assessed; by having appointed solely as a result of the exercise of one's voting rights a majority of the members of the administrative, management or supervisory bodies of the undertaking being assessed who have held office during the present and previous financial year; by controlling alone, pursuant to an agreement with other shareholders in or members of the undertaking being assessed, a majority of shareholders' or members' voting rights in that undertaking being assessed; by having the right to exercise a dominant influence over the undertaking being assessed, pursuant to an agreement entered into with that undertaking being assessed or to a provision in its Memorandum or Articles of Association, where the law governing that undertaking being assessed permits its being subject to such agreement or provision; by having the power to de facto exercise the right to exercise a dominant influence over the undertaking being assessed, without being the holder of that right; by having the right to use all or part of the assets of the undertaking being assessed; by managing the business of the undertaking being assessed on a unified basis, while publishing consolidated accounts; or by sharing jointly and severally the financial liabilities of the undertaking being assessed, or guaranteeing them.

PUBLIC

(73) Regulation (EU) No 654/2014 of the European Parliament and of the Council[31] enables the Union to suspend or withdraw concessions or other obligations under international trade agreements in order to respond to breaches by third countries of international trade rules that affect the Union's commercial interests. Any exercise of the Union's rights under Regulation (EU) 2021/167 should also be reflected in the interpretation of the definition of domestic ~~undertaking~~**entity** under this Regulation.

(74) In addition to challenges relating to the security of supply of ~~semiconductors~~**chips**, increasing attention has been drawn to cybersecurity risks associated with sourcing from certain suppliers for critical infrastructures, equipment or systems. Such cybersecurity risks should not fall within the scope of this declaration submitted by economic operators in procurement procedures involving the provision or use of ~~semiconductors~~**chips** and are governed by the applicable Union cybersecurity legal framework. Notwithstanding, economic operators are to ensure compliance with, and act in accordance with, relevant Union cybersecurity legislation.

(75) Given the complexity and evolving nature of semiconductor supply chains, the Commission, in consultation with the European Semiconductor Board and relevant industrial stakeholders, should, where necessary, issue recommendations identifying specific infrastructures, equipment or systems for which supply chain resilience is particularly important seeing potential supply chain risks, and such recommendations should be considered by contracting authorities and contracting entities in the preparation and conduct of procurement procedures, thereby supporting consistent implementation across the Union. **In developing such recommendations, due consideration should be given to the diversity of the semiconductor value chain and to specialised technologies and ecosystems present across different Member States.**

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[31] Regulation (EU) No 654/2014 of the European Parliament and of the Council of 15 May 2014 concerning the exercise of the Union's rights for the application and enforcement of international trade rules and amending Council Regulation (EC) No 3286/94 laying down Community procedures in the field of the common commercial policy in order to ensure the exercise of the Community's rights under international trade rules, in particular those established under the auspices of the World Trade Organization (OJ L 189, 27.6.2014, pp. 50-58, ELI: http://data.europa.eu/eli/reg/2014/654/oj).

(76) In order to preserve flexibility and avoid undue constraints on procurement procedures, contracting authorities and contracting entities should be allowed not to apply the requirement, including those relating to dual sourcing involving domestic ~~undertakings~~**entities** in duly justified cases, including where there is a lack of competition, absence of suitable tenderers, or where their application would lead to disproportionate costs or technical incompatibilities. Such derogations should be interpreted narrowly and applied in a transparent manner, ensuring that the objectives of strengthening semiconductor supply chain resilience and safeguarding the functioning of critical entities are not undermined.

(77) In order to ensure the effective and consistent application of measures aimed at strengthening the resilience and security of semiconductor supply in public procurement, the Commission may provide guidance and facilitate coordination among relevant actors. Such guidance should support the use of recommendations identifying infrastructures, equipment or systems for which ~~semiconductor~~**chip** supply by domestic ~~undertakings~~**entities** is particularly relevant, as well as the preparation and assessment of security of supply declarations, including elements related to supply chain mapping, the proportion of domestic ~~undertakings~~**entities** involved, resilience strategies such as dual sourcing, and vulnerability and risk assessments. The guidance should also facilitate the application of common methodologies for assessing supply chain risks, in particular in sectors exposed to heightened vulnerabilities, and promote the exchange of best practices and relevant information, with a view to ensuring a coherent approach across the Union and supporting the effective functioning of the internal market. **Such guidance should be proportionate and should avoid unnecessary administrative burdens, particularly for SMEs.**

PUBLIC

(78) In order to increase the transparency and safeguard the security of supply of ~~semiconductors~~**chips** for critical sectors, it is necessary to provide for the possibility of further Union action where the identified risks are not adequately addressed. Where, following consultation with the European Semiconductor Board, the Commission concludes that the measures recommended to contracting authorities or contracting entities to address such risks are insufficient, it should be empowered to adopt implementing decisions regarding which public authorities shall require economic operators to submit a security of supply declaration and for which procedures and products. **Such decisions should be based on objective evidence, respect the principles of necessity and proportionality, and take into account the specific characteristics of the sectors concerned.**

(78a) In order to ensure that security of supply declarations are targeted and proportionate to the procurement concerned, contracting authorities and contracting entities have flexibility to determine, where they require such a declaration, the chips incorporated into the infrastructure, equipment or system covered by the procurement for which information is relevant. A security of supply declaration should therefore not be understood as requiring information on all chips incorporated into the infrastructure, equipment or system concerned, but only on those specified by the contracting authority or contracting entity in the procurement documents. Where an implementing decision adopted pursuant to this Regulation specifies the infrastructures, equipment or systems for which a security of supply declaration is to be required, the Commission could further specify the type of chips in those infrastructures, equipment or systems in respect of which the declaration should provide information.

PUBLIC

(78b) **The overview of undertakings involved in the supply of the chips incorporated in the infrastructure, equipment or system concerned should be established on the basis of reasonable efforts by the economic operator. Economic operators preparing a security of supply declaration should not be required to obtain information on undertakings involved at every stage of the semiconductor supply chain where such information is not reasonably available to them or cannot reasonably be obtained. The information provided should therefore be limited to the level of detail that could reasonably be established, taking into account the information that is available or could be reasonably made available to the economic operator and the efforts required to obtain it, as well as the need to ensure that the information requested remains proportionate to the procurement concerned. Manufacturer declarations, supply-chain statements and equivalent documentation issued by direct suppliers should, for the purposes of the procurement procedure concerned, constitute sufficient evidence of the information provided, unless there are objective grounds to question its reliability. Such reliance should facilitate the preparation of security of supply declarations and avoid disproportionate administrative burdens. The acceptance of such information for the purposes of a procurement procedure should not, however, be construed as establishing a presumption of conformity with any requirements arising under other Union or national law, or as relieving the relevant economic operator or other person of any obligations applicable under such law.**

PUBLIC

(78c) **The information concerning the semiconductor supply chain resilience and diversification strategy of the tenderer should enable the contracting authority or contracting entity to assess the measures taken by the tenderer to reduce vulnerabilities arising from excessive concentration of sources of supply or production. Such information could concern, as appropriate to the procurement concerned, the geographic diversification of sources of supply or places of production, measures limiting dependency on a single third country or on a limited number of third countries where such dependency could give rise to vulnerabilities, the avoidance of undue reliance on a single economic operator or on a limited number of economic operators established in a third country, or the use of dual or multiple sourcing strategies. Where feasible and appropriate having regard to the subject matter of the procurement and the availability of suitable suppliers, such strategies could also include recourse to at least one domestic entity. The information requested should remain proportionate to the procurement concerned and should take into account the specific characteristics of the semiconductor supply chain concerned.**

(78d) **The notification of national competent authorities by contracting authorities and entities on the domestic entities identified in security of supply declarations is intended solely to enable the national competent authority to obtain information necessary for the application of this Regulation and should constitute an administrative obligation of the contracting authority or contracting entity. Failure to comply with that notification obligation should therefore not, as such, be subject to the penalties laid down in this Regulation. Nor should such failure, as such, constitute a ground for review, challenge or invalidation of a procurement decision under Council Directive 89/665/EEC or Council Directive 92/13/EEC. This should be without prejudice to any other legal remedies or consequences that may arise under Union or national law in respect of infringements of the applicable procurement rules.**

PUBLIC

(79) The semiconductor supply chain experiences disruptions that may damage certain downstream sectors economically. Critical sectors linked to public security, such as energy, defence or public administration, and those sectors where ~~semiconductors~~**chips** represent a large percentage of the value of the final product, such as automotive, datacentres or industrial automation, are particularly exposed to disruptions in semiconductor supply chains. Therefore, the Commission should have the possibility to identify them as risk-prone sectors. **The identification of risk-prone sectors should be based on objective criteria and should take into account the strategic importance of specialised sectors and technologies across the semiconductor value chain.**

(80) In order to clarify the necessary information to include, the Commission should, where appropriate, issue methodological guidance on how to carry out risk assessments that address the creation of a dual sourcing strategy, upstream and downstream supply chain mapping, and vulnerability analysis and sensitivity to supply disruption. For that purpose, the Commission may issue methodological recommendations on how to carry out risk assessments for those sectors. **Such guidance should remain technology-neutral, proportionate and adaptable to the specific characteristics of different sectors and semiconductor technologies.**

(81) In order to ensure a high level of resilience of the Union's semiconductor supply chain, it is necessary to provide for the possibility of further Union action where the identified risks are not adequately addressed. Where, following consultation with the European Semiconductor Board, the Commission concludes that the measures recommended to address such risks are insufficient, it should be empowered to adopt implementing decisions specifying appropriate risk mitigation measures. Such measures may include, where justified and proportionate, requirements for diversification of supply sources, including dual sourcing, or the building-up of strategic stocks. Those measures should be targeted, proportionate, and take into account the specificities of the sectors and companies concerned, as well as the need to preserve the functioning of the internal market and avoid undue administrative burden. The assessment of risks to the semiconductor supply chain should be based on objective and reliable evidence. For that purpose, the Commission should take into account, inter alia, publicly available information, data collected through requests for information, as well as indications of repeated or persistent supply chain disruptions. The use of such evidence should ensure that any measures adopted are well-founded, transparent, and proportionate to the identified risks, while safeguarding the confidentiality of sensitive business information. **Binding measures should be exceptional and should be adopted only after objective and reliable evidence demonstrates a serious risk to security of supply of Union significance and the ineffectiveness of recommendations, voluntary action and other less restrictive measures. Measures should be time-limited, subject to periodic review and take into account the technical and economic capabilities of undertakings, in particular SMEs, sector-specific circumstances and existing contractual commitments.**

(82) With the interest of continuity of supply and reliability in mind, contracting authorities and contracting entities are empowered to request risk assessments on the semiconductor supply chains of economic operators participating in public procurement or other public funding procedures that concern risk-prone sectors. **Such requests should be proportionate to the nature, scale and strategic relevance of the procurement concerned.**

/…/

PUBLIC

HAVE ADOPTED THIS REGULATION:

Chapter I
General provisions

Article 1

Subject matter

1. This Regulation establishes a framework for strengthening **and developing the competitiveness, indispensability, resilience and prosperity of the Union's**~~the~~ semiconductor ecosystem, and addressing and preventing dependencies that can threaten the security of supply of ~~semiconductors~~**chips** at Union level, in particular through the following measures:

   (a) the continuation and further development of the Chips for Europe Initiative, originally established under Regulation (EU) 2023/1781 and referred to in this Regulation as 'Chips for Europe Initiative 2.0;

   (b) setting the criteria to recognise and support European semiconductor technology initiatives that are first-of-a-kind initiatives and strategic projects ~~that foster the indispensability, resilience, and prosperity of the Union's semiconductor ecosystem~~;

   (c) enhancing the coordination mechanism between the Member States and the Commission originally established under Regulation (EU) 2023/1781 which concerns the mapping and monitoring **of** the Union's semiconductor ~~sector~~**value chain**, crisis prevention and response to ~~semiconductor~~**chip** shortages and, where relevant, requests for information and consultation with stakeholders ~~from~~**across** the semiconductor supply chain.

2. The first general objective of this Regulation is to ensure the conditions necessary for the competitiveness and innovation capacity of the Union in ~~semiconductor~~**chip** technologies and to ensure the adjustment of the industry to structural changes.

3. The second general objective, separate from and complementary to the first general objective set out in paragraph 2, is to enhance crisis preparedness to ensure the EU's security of supply thereby improving the functioning of the internal market by laying down a uniform Union legal framework for increasing the Union's **competitiveness,** indispensability, resilience and prosperity in the field of ~~semiconductor~~**chip** technologies.

4. This regulation shall apply without prejudice to the specific procurement procedures and qualification standards applicable in the defence sector referred to in Regulation (EU) 2025/2643.

Article 2

Definitions

For the purposes of this Regulation, the following definitions apply:

(1) 'semiconductor' means one of the following:

(a) a material, including advanced materials, either elemental or compound, whose electrical conductivity can be modified;

(b) component consisting of a series of layers of semiconducting, insulating and conducting materials defined according to a predetermined pattern, and intended to perform well-defined electronic or photonic functions or both;

(2) 'chip' means ~~an electronic device comprising various functional elements on a single piece of semiconductor material, typically taking the form of memory, logic, processor, optoelectronics and analogue devices;~~**one of the following:**

(a) an electronic device comprising a single or various functional elements on one or several pieces of semiconductor material, typically taking the form of memory, logic, processor, optoelectronics and analogue devices;

(b) a photonic integrated circuit;

(c) a quantum chip;

(2a) **'photonic integrated circuit' means a device comprising a single or various functional elements on a single chip or a substrate that generate, guide, manipulate, process, or detect light;**

(3) 'quantum chip' means a **chip-level** device that ~~processes~~**incorporates quantum components, structures, or interfaces for generating, manipulating, controlling, processing, storing, transmitting or measuring quantum states or quantum** information ~~at the level of individual quantum systems, with a varying level of component integration on-chip depending on the quantum platform used, including platforms for quantum computing, communication, sensing or metrology~~;

(4) 'technology node' means a specific semiconductor manufacturing process and its design rules;

(5) 'semiconductor supply chain' means the system of activities, organisations, actors, technology, information, resources and services involved in the production of ~~semiconductors~~**chips**, including raw and processed materials, such as gases, ~~semiconductor~~**chip** manufacturing equipment, design, including related software development, fabrication, assembly, testing and packaging;

(6) 'semiconductor value chain' means the set of activities in relation to a ~~semiconductor~~**chip** product from its conception to its end use, including raw and processed materials, such as gases, ~~semiconductor~~**chip** manufacturing equipment, research, development and innovation, design, including related software development, fabrication, testing, assembly and packaging**, including advanced packaging,** to embedding and integration in end products, as well as end-of-life processes, such as reuse, disassembly and recycling;

(7) 'pilot line' means a testing and experimentation facility **or facilities** addressing higher technology readiness levels up to industrial uptake to test, demonstrate, validate and calibrate products, equipment, **materials,** processes or systems;

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(7a) 'pilot testbed' means a facility or infrastructure for the integration, demonstration, testing and validation of innovative semiconductor technologies or products, including their integration into systems and in combination with other technologies or components, in conditions representative of their intended use in key applications or user industries, with a view to validating their performance, feasibility and readiness for industrial deployment;

(8) 'small and medium-sized enterprises' or 'SMEs' means small or medium-sized enterprises as defined in the Annex to Commission Recommendation 2003/361/EC[32];

(9) 'small mid-cap' means small mid-cap as defined in the Annex of Recommendation 2025/1099/EC;

(9a) 'research and knowledge-dissemination organisation' means an entity (such as universities or research institutes, technology transfer agencies, innovation intermediaries, research-oriented physical or virtual collaborative entities), irrespective of its legal status (organised under public or private law) or way of financing, whose primary goal is to independently conduct fundamental research, industrial research or experimental development or to widely disseminate the results of such activities by way of teaching, publication or knowledge transfer;

(10) 'first-of-a-kind initiative' means any of the following initiatives **in the semiconductor value chain**, which provides innovation in the Union with regard to the manufacturing process or final product to the extent that this innovation is not yet sufficiently present or committed to be built within the Union to ensure the Union's resilience and security of supply, including innovation that concerns improvements in computing power or in the level of security, safety or reliability, energy and environmental performance, the technology node or substrate materials, or in the implementation of production processes that lead to efficiency gains, or improves recyclability, or reduces production inputs:

(a) a new or substantially upgraded ~~semiconductor~~**chip** manufacturing facility;

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[32] Commission Recommendation of 6 May 2003 concerning the definition of micro, small and medium-sized enterprises (notified under document number C(2003) 1422) (OJ L 124, 20.5.2003, p. 36, ELI: http://data.europa.eu/eli/reco/2003/361/oj).

(b) a new or substantially upgraded facility or process for the production of equipment;

(c) a new or substantially upgraded facility or process for the production of key components for such equipment or other production of inputs predominantly used in ~~semiconductor~~**chip** manufacturing, such as materials;

(d) a new or substantially upgraded facility for electronics manufacturing or integration;

(e) new **or substantially upgraded** manufacturing-centred chip design activities;

(11) 'manufacturing-centred chip design activities' means the preparation of designs for fabrication, design–process co-optimisation, and the execution of final tape-out, being the stage at which a chip design is committed to fabrication in the form of a physical prototype for validation prior to volume production;

(12) 'next-generation ~~semiconductor~~**chip** technologies' means ~~semiconductor~~**chip** technologies that go beyond the state of the art in offering significant improvements in functional performance, computing power or energy efficiency as well as other significant energy and environmental gains;

(13) 'cutting-edge ~~semiconductor~~**chip** technologies' means state-of-the-art innovation in chips and semiconductor technologies when the projects are carried out;

(14) 'semiconductor manufacturing' means any of the stages of production and processing of ~~semiconductor~~**chip** wafers **or substrates**, including design, substrate materials, front-end and back-end, necessary to deliver a finished ~~semiconductor~~**chip** product;

(15) 'front-end' means the entire processing of a ~~semiconductor~~ wafer **resulting in chips**;

(16) 'back-end' means the packaging, **including advanced packaging,** assembly and test of a ~~semiconductor~~ product **based on chips**;

(17) 'electronics manufacturing and integration' means the manufacturing or integration of printed circuit boards, advanced packaging substrates and electronic manufacturing concerning the assembly, testing or system integration of ~~semiconductors or semiconductor based~~**chips or chip-based** products;

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(18) ‘user of ~~semiconductors~~**chips**’ means an undertaking that produces products in which ~~semiconductors~~**chips** are incorporated;

(19) ‘key market actors’ means undertakings in the Union’s semiconductor supply chain, the reliable functioning of which is essential for the supply of ~~semiconductors~~**chips**;

(20) ‘critical sector’ means any sector referred to in Annex V;

(21) ‘crisis-relevant product’ means any of the following products that are affected by a semiconductor crisis and relevant to ensure crucial functions of a critical sector:

(a) ~~semiconductors or~~ chips which are either deployed directly by critical sectors or used in order to produce devices used by critical sectors;

(b) intermediate products required to produce ~~semiconductors or~~ chips;

(c) raw and processed materials required to produce ~~semiconductors or~~ chips or intermediate products.

(22) ‘production capability’ means the ability of a facility to produce certain types of products;

(23) ‘production capacity’ means the maximum potential output of a facility;

(24) ‘trade secret’ means a trade secret as defined in Article 2, point (1), of Directive (EU) 2016/943;

(25) ‘permit-granting procedure’ means a process that covers all relevant permits to build, expand, convert and operate industrial ~~semiconductor~~**chip** manufacturing projects, including building, chemical and grid connection permits as defined in Article 1 of [the Proposal for a Directive amending Directives (EU) 2018/2001, (EU) 2019/944, (EU) 2024/1788 as regards acceleration of permit-granting procedures], and environmental assessments and authorisations where required, and encompassing all applications and procedures from the acknowledgement that the application is complete to the notification of the ~~comprehensive~~ decision on the outcome of the procedure;

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(26) ‘contract’ means public contracts as defined in Article 2(1), point (5), of Directive 2014/24/EU, supply, works and service contracts as defined in Article 2, point (1), of Directive 2014/25/EU of the European Parliament and of the Council [insert footnote], and concession contracts as defined in Article 5, point (1), of Directive 2014/23/EU of the European Parliament and of the Council;

(27) ‘contracting authority’ means, a contracting authority as defined in Article 6 of Directive 2014/23/EU, Article 2(1), point (1), of Directive 2014/24/EU and Article 3 of Directive 2014/25/EU;

(28) ‘contracting entity’ means a contracting entity as defined in Article 7 of Directive 2014/23/EU and Article 4 of Directive 2014/25/EU;

(29) ‘secure processing environment’ means the physical or virtual environment and organisational means to ensure compliance with Union law, including Regulation (EU) 2016/679 of the European Parliament and of the Council[33], in particular with regard to data subjects’ rights, antitrust rules, IP rights and commercial and statistical confidentiality, integrity and accessibility, as well as with applicable national law, and to allow the entity providing the secure processing environment to determine and supervise all data processing actions, including the display, storage, download and export of data and the calculation of derivative data through computational algorithms;

(30) ‘legal representative’ means a natural or legal person domiciled or established in the Union and designated to act on behalf of the Platform established in accordance with Article 34 of this Regulation;

(31) ‘domestic ~~undertaking~~**entity**’ means:

(a) any ~~undertaking~~**entity** in the semiconductor value chain that ~~has its seat in the Union and~~ is under the ownership and control of a Union ~~undertaking~~**entity, or**;

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[33] Regulation (EU) 2016/679 of the European Parliament and of the Council of 27 April 2016 on the protection of natural persons with regard to the processing of personal data and on the free movement of such data, and repealing Directive 95/46/EC (General Data Protection Regulation) (OJ L 119, 4.5.2016, p. 1, ELI: http://data.europa.eu/eli/reg/2016/679/oj).

(b) any ~~undertaking~~**entity** in the semiconductor value chain which fulfils ~~one~~**any** of the following criteria~~, regardless of whether its seat is in the Union~~:

~~(c) it is owned and controlled by a Union undertaking, and has its seat outside the Union;~~

~~(d)~~**(ii)** it is owned and controlled by an ~~undertaking~~**entity** established in a third country or territory with which the Union has concluded an agreement establishing a free trade area, a customs union, or a strategic partnership on semiconductors concluded in accordance with Article ~~49~~**47**;

~~(e)~~**(iii)** it is owned and controlled by an ~~undertaking~~**entity** established in a signatory of the WTO Agreement on Government Procurement.

(iv) it is an Integrated Production Facility or the Open European Foundry under Regulation (EU) 2023/1781, or is a European semiconductor technology initiative or a strategic project under this Regulation, and has not experienced a change in ownership or control since being awarded such status;

(32) 'ownership' means being in **ultimate** possession of 50% or more of the proprietary rights of a legal person, entity or body, or having a majority interest therein;

(33) 'control' means control as defined in Article 2(6) of Regulation (EU) 2021/697;

(34) 'Union ~~undertaking~~**entity**' means an ~~undertaking~~**entity** established under the laws of a Member State;

(35) 'strategic partnership on semiconductors' means a commitment between the Union and a third country or territory **concluded in accordance with Article 47** to increase cooperation related to the semiconductor value chain that is established through a non-binding instrument setting out concrete actions of mutual interest;

(35a) 'European semiconductor technology initiative' means a chip project carried out by domestic entities qualifying as a first-of-a-kind initiative in accordance with this Regulation and which is voluntarily submitted for recognition by the Commission with a view to giving visibility to European initiatives that contribute to the competitiveness, indispensability, resilience and prosperity and security of supply of the Union's chip ecosystem and comply with the requirements laid down in Article 14;

(36) 'strategic project' means a project **in the field of chip technology** that provides significant added value to the Union by substantially contributing to **the** objectives of **this Regulation and thus to the** common Union interest, ~~have~~**has** a clear cross-border dimension, in particular through technical **or operational** cooperation or public support involving more than one Member ~~States~~**State**, and contributes to strengthening the **competitiveness,** indispensability, resilience and prosperity of the Union's ~~semiconductor value chain~~**chip ecosystem** and the Union's technological sovereignty and technological leadership by enabling, advancing or securing critical capacities, technologies or capabilities within the Union, including by reducing strategic dependencies~~.~~**;**

(37) 'Chips Joint Undertaking' means the joint undertaking established by Council Regulation (EU) 2021/2085 and, where applicable, any **potential** successor entity or initiative established under Union law pursuant to a subsequent Multiannual Financial Framework.

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Chapter II

Chips for Europe Initiative 2.0

Article 3

Chips for Europe Initiative 2.0

1. The Chips for Europe Initiative 2.0 shall be supported for the duration of the Multiannual Financial Framework 2021-2027, established by Council Regulation (EU, Euratom) 2020/2093[34].

2. The Chips for Europe Initiative 2.0 shall be supported by funding from Horizon Europe and the Digital Europe Programme in accordance with Regulations (EU) 2021/694 and (EU) 2021/695, as well as by national and private funding.

2a. The amount of the Union support under paragraph 2 shall be established in accordance with the rules of the Horizon Europe and the Digital Europe Programme as part of the annual budgetary procedure, subject to the availability of funding. The budgetary authority shall determine the appropriations available each year. Funding may also be made available from the general budget of the Union.

Article 4

Objective of the Chips for Europe Initiative 2.0

1. The general objective of the Chips for Europe Initiative 2.0 shall be to achieve large-scale technological capacity building **in the Union** and support related research and innovation activities throughout the Union's semiconductor value chain, in order to:

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[34] Council Regulation (EU, Euratom) 2020/2093 of 17 December 2020 laying down the multiannual financial framework for the years 2021 to 2027 (OJ L 433I, 22.12.2020, p. 11, ELI: http://data.europa.eu/eli/reg/2020/2093/oj).

(a) strengthen the Union's technological sovereignty, economic security, resilience, prosperity, indispensability and industrial competitiveness, by **building on and ensuring the continuity, where appropriate, of existing capacities and investments and by** providing for the transfer and industrial uptake of technologies developed under the Chips for Europe Initiative 2.0 **across the Union**;

(b) stimulate the Union's demand for ~~semiconductors~~**chips**, including through procurement procedures that promote, in accordance with Union law and international obligations of the Union, the uptake and integration of ~~semiconductor~~**chip** technologies, components and systems designed, developed or manufactured within the Union;

(c) enable the innovation, development and deployment of cutting-edge ~~semiconductor~~**chip** technologies~~, including photonics as a transversal and enabling technology~~, in particular those critical for artificial intelligence (AI), including edge AI, and for key application sectors such as health, energy, industrial automation, robotics, transport, defence, automotive**, aeronautics and aerospace** ~~and aeronautical systems~~, and data centres and cloud infrastructure**, while maintaining the Union's resilience and security of supply of mainstream semiconductor technologies**;

(d) contribute to the achievement of the green and digital transitions, in particular by reducing the energy, environmental and climate impact of electronic systems, improving the sustainability of next-generation chips and strengthening the circular economy processes, contribute to quality jobs within the semiconductor ecosystem, and address security-by-design principles which provide protection against cybersecurity threats.

2. The Chips for Europe Initiative 2.0 shall have the following six operational objectives:

(a) operational objective 1: supporting advanced design capacities for ~~semiconductor~~**chip** technologies;

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(b) operational objective 2: enhancing existing and developing new advanced pilot lines across the Union to enable development and industrial deployment of cutting-edge and next-generation ~~semiconductor~~**chip** technologies, and pilot testbeds to validate and demonstrate the integration and use of those technologies in key applications and user industries;

(c) operational objective 3: building advanced technology and engineering capacities for accelerating the innovative development of **next-generation and** cutting-edge quantum chips and associated semiconductor technologies;

(d) operational objective 4: supporting a network of competence centres across the Union by enhancing existing or creating new facilities**, as outlined in Article 6**;

(e) operational objective 5: building and strengthening advanced design, prototyping, and industrial deployment capacities for photonic integrated circuit technologies and other photonic technologies across the Union;

(f) operational objective 6: undertaking activities, to be described collectively as 'Chips Fund' activities, to facilitate access to finance, including by providing clear guidance, in particular for start-ups, scale-ups, SMEs and small mid-caps ~~in~~**across** the semiconductor value chain, through financial instruments and investment support mechanisms supporting equity, debt or blended finance under the European Innovation Council Accelerator, **the** InvestEU Fund and, where applicable, other Union instruments ~~and, if applicable, their successors under the Multiannual Financial Framework 2028-2034~~.

3. The Chips for Europe Initiative 2.0 shall support large-scale, cross-sectoral initiatives addressing major technological and industrial challenges of strategic relevance for the Union ('grand challenges').

4. The Chips for Europe Initiative 2.0's operational objectives may include capacity building activities and related research and innovation activities. Under the 2021-2027 Multiannual Financial Framework, all capacity building activities shall be financed through the Digital Europe Programme and the related research and innovation activities shall be funded through Horizon Europe.

Article 5

Operational objectives of the Chips for Europe Initiative 2.0

The Chips for Europe Initiative 2.0 shall:

(a) under its operational objective 1:

(i) maintain and extend a virtual design platform, available across the Union, integrating a wide range of new and existing design assets, tools and services, facilitating **fair** access, in particular, for ~~academia,~~ start-ups, scale-ups ~~and SMEs~~**, SMEs, small mid-caps, research and knowledge-dissemination organisation**, with a view to strengthening the growth and scale-up of fabless undertakings in the Union;

(ii) extend the Union's design capabilities, including in photonics and quantum technologies, by fostering innovative developments in advanced chip design and architectures, and, to that end, support ~~ambitious strategic design~~ projects **that significantly advance Union chip design capabilities, address critical technological or supply dependencies and are** of high relevance to the Union's strategic autonomy and competitiveness;

(b) under its operational objective 2:

(i) strengthen capabilities in next-generation chip production technologies and semiconductor manufacturing equipment, by integrating research and innovation activities and preparing the development of future technology nodes and semiconductor manufacturing processes;

(ii) support innovation at a large scale through access to new or existing pilot lines for experimentation, test, process control, final device characterisation, testing and validation of new technologies and design concepts integrating key functionalities;

(iii) support innovation through access to new or expanded pilot testbeds where different innovative technologies or products are combined and integrated for the development and validation of new devices in key applications and user industries before full industrial-scale deployment, in order to identify risks, validate performance, and ensure feasibility in real-world conditions;

(iv) provide support to European semiconductor technology initiatives through preferential access to ~~new or existing~~ pilot lines, as well as ensure **effective** access on fair **and transparent** terms to ~~new~~ pilot lines and pilot testbeds for a wide range of users of the Union's semiconductor ecosystem;

(v) prepare for the transfer and industrial uptake of technologies developed under this operational objective **through measures included in this Regulation**;

(c) under its operational objective 3:

(i) support the development of ~~new or existing~~ pilot lines, clean rooms and foundries for prototyping and ~~producing~~**manufacturing** quantum chips for the integration of quantum circuits and control electronics;

(ii) develop facilities for testing and validating advanced quantum chips ~~produced~~**manufactured** by the pilot lines, with a view to closing the innovation feedback loop ~~between~~**with** designers, ~~producers~~**manufacturers** and users of quantum components;

(iii) develop innovative design libraries for quantum chips in close relation with operational objective 1;

(d) under its operational objective 4:

(i) ~~strengthen capacities and~~ offer a wide range of expertise **and support** to stakeholders, including end-user start-ups, scale-ups ~~and~~**,** SMEs, **small mid-caps, research and knowledge-dissemination organisations** and facilitating access to and the effective use of the capacities and facilities referred to in this Article;

(ii) address the knowledge and skills shortage and mismatch by attracting, mobilising, and retaining new talent on research, design, **testing and manufacturing,**~~and production~~ including reskilling and upskilling of workers;

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(e) under its operational objective 5:

(i) strengthen capabilities in production technologies, semiconductor manufacturing equipment and materials platforms for photonic integrated circuits by integrating research and innovation activities;

(ii) strengthen existing and develop new pilot lines and open-access semiconductor manufacturing facilities for the prototyping and ~~production of photonic integrated circuits and associated~~**manufacturing of relevant** photonic technologies;

(iii) develop and maintain design libraries and design automation tools for photonic integrated circuits, associated photonic technologies, and methods for their integration into modules available on open and non-discriminatory terms across the Union;

(iv) prepare for the transfer and industrial uptake of technologies developed under this operational objective **through measures included in this Regulation**;

(f) under its operational objective 6:

(i) provide support to start-ups ~~and~~**,** scale-ups**, SMEs and small mid-caps** across the semiconductor value chain in accessing finance at all stages of growth, with a particular focus on bridging the financing gap that prevents them from achieving the scale necessary to compete globally;

(ii) accelerate and improve accessibility to investment in the semiconductor value chain, in particular by mobilising venture capital and growth equity, and leverage funding from both the public and the private sectors, while increasing the **competitiveness,** indispensability, resilience and prosperity of the semiconductor ecosystem in the Union.

Those objectives shall be implemented, where appropriate, in accordance with the technical description set out in Annex I.

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Article 6

European network of competence centres in semiconductors

1. For the purposes of the Chips for Europe Initiative 2.0's operational objective 4, the European network of competence centres in semiconductors, system integration and design (the 'network') established under the Regulation (EU) 2023/1781 shall **continue to** be supported. The network shall be composed of the **competence centres already selected by the Chips Joint Undertaking and any additional** competence centres selected by the Chips Joint Undertaking in accordance with paragraph 3.

2. Competence centres shall perform all or some of the following activities to the benefit of and in close cooperation with the Union industry, in particular **start-ups, scale-ups,** SMEs and **small** mid-caps, as well as research and ~~technology~~**knowledge-dissemination** organisations~~, universities~~, and the public sector and other relevant stakeholders across the semiconductor value chain:

   (a) ensuring alignment between the activities of the competence centre and, where applicable, the semiconductor strategy of the Member State in which the competence centre is established**, while supporting the integration of the Member State's semiconductor strategy into the wider Union semiconductor ecosystem**;

   (b) raising awareness and providing the necessary know-how, expertise and skills to the stakeholders for helping them accelerate the development of new ~~semiconductor~~**chip** technologies, semiconductor manufacturing, equipment, design options and system concepts as well as the integration of new ~~semiconductor~~**chip** technologies, by using effectively the infrastructure and other available resources of the network;

   (c) ~~providing~~**supporting users in accessing, including cross-border** access ~~to~~**,** design services and design tools under the Chips for Europe Initiative 2.0's operational objective 1, as well as to the pilot lines supported under the Chips for Europe Initiative 2.0's operational objective 2;

   (d) raising awareness and providing or ensuring access to expertise, know-how and services, including system design readiness, ~~new and existing~~**the** pilot lines and supporting actions necessary to build skills and competences supported by the Chips for Europe Initiative 2.0;

(e) facilitating **collaboration and** the transfer of expertise and know-how between Member States and regions encouraging exchanges of skills, knowledge and good practices and encouraging joint programmes;

(f) developing and managing specific training, skilling and reskilling actions on ~~semiconductor~~**chip** technologies and their applications to support the development of the talent pool, as well as to increase the number of students and the quality of education in relevant fields of ~~studies~~**study**, at schools**, vocational education and training institutions** and universities ~~located in the Union~~, up to doctoral level**, located in the Union**;

(g) facilitating connections between students and ~~semiconductor~~**chip** undertakings across the Union, while paying particular attention to women's participation and underrepresented groups and building on existing initiatives which support education or training, or both, and mobility of students and workers within and from outside the Union.

3. Member States ~~shall~~**may** designate **additional** candidate competence centres in accordance with their national procedures, administrative and institutional structures through an open and competitive process.

The work programme of the Chips Joint Undertaking shall set the procedure for supporting the competence centres forming the network, including the selection criteria **for additional competence centres** as well as further details on the implementation of the tasks and functions referred to in this Article

The Chips Joint Undertaking shall select ~~the~~**any additional** competence centres ~~forming~~**to join** the network.

Member States and the Commission shall maximise synergies with existing competence centres established under other Union initiatives such as the European Digital Innovation Hubs referred to in Regulation (EU) 2021/694.

4. The competence centres shall have substantial overall autonomy to lay down their organisation, composition and working methods. The organisation, composition and working methods of the competence centres shall comply with and contribute to the objectives of this Regulation and the Chips for Europe Initiative 2.0.

Article 7

Grand challenges

1. Grand challenges shall develop, integrate, and ensure industrial deployment of promising and critical ~~semiconductor~~**chip** and related technologies of key importance for the Union, and be implemented **in accordance with Article 12(1) and**, where appropriate, in accordance with the technical description set out in Annex I.

2. The Chips for Europe Initiative 2.0 shall support grand challenges by:

~~(b)~~**(-a)** addressing major roadblocks in the further development of semiconductor technologies, such as miniaturisation, energy efficiency, sustainability, **new functionalities,** heterogeneous integration, security and reliability, and manufacturability~~.~~**;**

(a) promoting advanced R&D that will allow **the Union** to lead the next generation of AI **and quantum** chips, to sustain cloud, data centres and edge AI infrastructures through unprecedented energy efficiency levels, to secure Union capacities in ~~leading-edge~~**next-generation and cutting-edge chip** technologies, and to increase the Union's ~~semiconductor~~**chip design,** manufacturing **and integration** strengths;

~~(b) addressing major roadblocks in the further development of semiconductor technologies, such as miniaturisation, energy efficiency, sustainability, heterogeneous integration, security and reliability, and manufacturability.~~

(c) enlarging the semiconductor ecosystem **across the Union** by closely collaborating with vertical market sectors;

(d) achieving **and maintaining** a competitive edge in specific applications critical to the Union's technological sovereignty and industrial competitiveness by structuring collaboration between ~~semiconductor~~**chip** developers ~~and~~**,** user industries **and other relevant stakeholders**;

(e) integrating the efforts of multiple pilot lines and gearing them towards industrial usage through increased energy efficiency and advanced ~~semiconductor~~**chip** capabilities;

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(f) ensuring the transfer and industrial uptake of technologies developed under the Chips for Europe Initiative 2.0, including activities aimed at technology maturation, qualification, prototyping, **testing, validation,** demonstration, first industrial deployment, and transfer into production environments.

3. Grand challenges shall be implemented in coordination with grand challenges as established under Regulation (EU) XXXX/XXXX [the Cloud and AI Development Act (CADA)], as well as with initiatives undertaken by the European ~~High Performance~~**High Performance** Computing Joint Undertaking established by Council Regulation (EU) 2021/1173[35].

*Article ~~97~~**a***

Demand forum

1. The Commission shall set up a demand forum to **allow industrial users of semiconductor technologies to express their needs and** facilitate the showcase of semiconductor technologies **by relevant stakeholders**, in particular by European semiconductor technology initiatives and strategic projects, as well as integrated production facilities and open EU foundries recognised under Regulation (EU) 2023/1781 in accordance with competition rules.

2. The demand forum shall be implemented by the Industrial Alliance for Semiconductors**, facilitating participation of relevant stakeholders from across the semiconductor value chain**. **The European Semiconductor Board shall be kept regularly updated on the activities in the demand forum.**

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35 Council Regulation (EU) 2021/1173 of 13 July 2021 on establishing the European High Performance Computing Joint Undertaking and repealing Regulation (EU) 2018/1488 (OJ L 256, 19.7.2021, p. 3, ELI: http://data.europa.eu/eli/reg/2021/1173/oj).

Article 8

Demand accelerators

1. ~~The Commission and Member States~~**Demand accelerators** shall stimulate the uptake of ~~semiconductors~~**chips** designed or manufactured within the Union, in particular in **the** key markets ~~such as cloud, automotive, aeronautical, telecom, defence,~~**set out in Annex VI** and, where appropriate, in ~~others~~**other markets**.

2. ~~The~~ Demand accelerators shall be implemented by the Industrial Alliance for Semiconductors **through thematic working groups**.

3. **For the purposes of paragraph 1, demand accelerators shall**~~The Commission may~~, in cooperation with **the Commission and** Member States**, as well as** ~~and~~ relevant industrial stakeholders**, including start-ups, scale-ups, SMEs and small mid-caps**, and in accordance with competition rules:

   (a) facilitate potential users, in particular off-takers of ~~semiconductor~~**chip** technologies, to discuss requirements and technological specifications of the ~~semiconductor-related~~**chip-related** products **and solutions** that their ~~industry is~~**industries are** likely to require~~.~~**;**

   (b) enable the development of common technical roadmaps, and support and stimulate co-design activities between ~~semiconductor~~**chip designers, chip** manufacturers ~~established in the Union~~**, equipment manufactures** and downstream industrial users, including system integrators ~~and equipment manufacturers~~**, that are established in the Union**, with the aim of developing ~~semiconductor~~**chip** components tailored to Union industrial applications;

   (c) facilitate collaborative platforms, pilot projects or design partnerships enabling early involvement of industrial users in the design**, testing, validation and deployment** of innovative ~~semiconductor~~**chip** technologies developed in the Union.

3a. Member States shall endeavour to promote the participation of their industrial stakeholders in the demand accelerators.

PUBLIC

~~*Article 9*~~

~~**Demand forum**~~

~~1. The Commission shall set up a demand forum to facilitate the showcase of semiconductor technologies, in particular by European semiconductor technology initiatives and strategic projects, as well as integrated production facilities and open EU foundries recognised under Regulation (EU) 2023/1781 in accordance with competition rules.~~

~~2. The demand forum shall be implemented by the Industrial Alliance for Semiconductors.~~

Article 10

Support for chip innovation procurement

1. ~~For the purposes of supporting~~**The Chips Joint Undertaking shall support** contracting authorities or contracting entities and economic operators acting as purchasing entities in ~~the~~**innovation** procurement~~, integration, qualification and first deployment of systems integrating semiconductors the Chips Joint Undertaking and shall undertake~~ **with** the following actions:

   (a) support ~~the formation, where relevant, of cross-border joint~~**innovation** procurement ~~arrangements between contracting authorities or contracting entities~~**aimed at the integration, qualification and first deployment of systems integrating innovative chip technologies**;

   (b) support the integration**, qualification and first** ~~and~~ deployment of innovative **chip technologies across the entire** semiconductor **value chain, including those** technologies~~.~~ **developed within the Chips for Europe 2.0 initiative, including, where appropriate, activities necessary for their adoption, such as redesign, testing and validation;**

   (ba) facilitate access to technical expertise, infrastructure and support services necessary for the integration, testing, validation and qualification of innovative chip technologies and systems integrating such technologies prior to their first deployment;

(bb) support, where relevant and on a voluntary basis, cooperation between contracting authorities or contracting entities from different Member States, including through the formation of buyer groups and cross-border joint procurement arrangements.

1a. The support referred to in paragraph 1 shall be provided without prejudice to the responsibility of contracting authorities, contracting entities or purchasing entities for the preparation and conduct of their procurement procedures and the award of contracts, in accordance with applicable international, Union and national law.

Article 11

Synergies with other programmes

1. The Chips for Europe Initiative 2.0 shall be implemented in synergy with Union programmes in accordance with Annex IV~~.~~**, as well as in close coordination with national semiconductor strategies and programmes of the Member States.** The Commission shall ensure that the achievement of the objectives of the Chips for Europe Initiative 2.0 referred to in Article 4 is not hampered when leveraging the complementary character of the Chips for Europe Initiative 2.0**, facilitating coordination and coherence** with Union programmes.

Article 12

Implementation

1. The Chips for Europe Initiative 2.0's operational objectives 1 to 5 and grand challenges shall be entrusted to the Chips Joint Undertaking and implemented by actions set out in its work programme **governed by the programme rules of Regulation (EU) 2021/694 and Regulation (EU) 2021/695**.

2. In order to reflect technological change and market developments relevant to the semiconductor ~~sector~~**value chain**, the Commission is empowered to adopt delegated acts in accordance with Article 55 to amend Annex I with regard to the actions set out therein in a manner consistent with the objectives of the Chips for Europe Initiative 2.0 as set out in Article 4.

3. In order to ensure effective implementation and evaluation of the Chips for Europe Initiative 2.0 and to reflect technological change and market developments, the Commission is empowered to adopt delegated acts in accordance with Article 55 to amend Annex III with regard to the measurable indicators to monitor the implementation and to report on the progress of the Chips for Europe Initiative 2.0 towards the achievement of its objectives as set out in Article 4.

4. In order to ensure effective implementation, monitoring and evaluation of the Chips for Europe Initiative 2.0, the annual activity report of the Chips Joint Undertaking shall include information on matters related to the Chips for Europe Initiative 2.0's operational objectives 1 to 5 and grand challenges, on the basis of the measurable indicators set out in Annex III.

5. The Commission shall **on a regular basis** inform the European Semiconductor Board on progress in the implementation of **and participation in** the Chips for Europe Initiative 2.0's operational objective 6 ~~on a regular basis~~.

Chapter III
Security of supply and demand

SECTION 1
SEMICONDUCTOR MANUFACTURING CAPABILITIES

Article 13

Public interest and public support

1. European semiconductor technology initiatives and strategic projects shall be considered to contribute to the security of supply of ~~semiconductors and the~~**chips and to the competitiveness, indispensability,** resilience **and prosperity** of the Union's semiconductor ecosystem and therefore to be in the public interest.

2. In order to ~~reach~~**enhance** security of supply and the **competitiveness, indispensability,** resilience **and prosperity** of the Union's semiconductor ecosystem, Member States may, without prejudice to Articles 107 and 108 TFEU, apply support measures and provide for administrative support to strategic projects in accordance with Regulation (EU) XXXX/XXXX [European Competitiveness Fund] and other relevant Union legislation and European semiconductor technology initiatives-.

3. Furthermore, the Commission may apply support measures, including but not limited to grants, to strategic projects **across the entire semiconductor value chain** in accordance with Regulation (EU) XXXX/XXXX [European Competitiveness Fund] and other relevant Union legislation.

Article 14

European semiconductor technology initiatives

1. European semiconductor technology initiatives shall be carried out by domestic ~~undertakings~~**entities**.

2. European semiconductor technology initiatives shall demonstrate that they will articulate their supply chain in a way that reduces supply chain dependence on non-domestic ~~undertakings~~**entities** and strengthen the Union's security of supply.

3. European semiconductor technology initiatives shall be first-of-a-kind initiatives that contribute to the **competitiveness,** indispensability, resilience and prosperity and security of supply of the Union's semiconductor ecosystem.

4. At the time of submitting an application in accordance with Article 15(1) a European semiconductor technology initiative shall be required to qualify as first-of-a-kind initiative.

5. First-of-a-kind initiatives do not have to be a recipient of support measures or administrative support as referred to in Article 13 to apply for the status of European semiconductor technology initiative.

6. A European semiconductor technology initiative shall comply with the following requirements:

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(a) its establishment has a clear positive impact with spill-over effects beyond itself or the Member State or Member States concerned, **including through cooperation with actors across the semiconductor value chain in other Member States,** on the Union's semiconductor value chain and the Union's end markets in the medium to long term, with a view to ensuring **competitiveness,** indispensability, resilience and prosperity of the semiconductor ecosystem, including the growth of start-ups and SMEs, and contributing to the Union's green and digital transitions, and where relevant to the business model of the facility, taking into account the extent to which it offers front-end or back-end production capacity, or both, to undertakings which are not related to the facility, if there is sufficient demand;

(b) it provides an assurance that it is not subject to the extraterritorial application of public service obligations of third countries in a way that may undermine the undertaking's ability to comply with the obligations set out in Article 43(1) and commits to informing the Commission when such obligation arises;

(c) it invests in the Union in continued innovation with a view to achieving concrete advances in ~~semiconductor~~**chip** technology or preparing next-generation ~~semiconductor~~**chip** technologies;

(d) it supports the Union's talent pipeline by developing and deploying **specialised** educational and skills training ~~and by increasing the pool of qualified and skilled workforce~~**, such as in close cooperation with the competence centres and other relevant stakeholders**;

(e) if it is a production facility, it participates in the Business-to-Business Semiconductor Supply Chain Platform as referred to in Article 34.

7. For the purposes of investing in continued innovation in accordance with paragraph 6, point (c)**,** of this Article, European semiconductor technology initiatives shall have preferential access to the pilot lines established in accordance with Article 5, point (b). Any such preferential access shall neither exclude nor prevent effective **and transparent** access on fair terms to the pilot lines ~~by other interested undertakings~~**for a wide range of users of the Union's semiconductor ecosystem**, in particular start-ups**, scale-ups, SMEs and small mid-caps** ~~and SMEs~~.

8. Where a European semiconductor technology initiative offers production capacity to undertakings not related to the initiative, the initiative shall establish and maintain adequate and effective functional separation of the design and ~~semiconductor~~**chip** manufacturing processes in order to ensure the protection of information obtained at each stage.

Article 15

Application for status as European semiconductor technology initiative

1. Any undertaking or any consortium of undertakings may submit**, at any time,** an application to the Commission to grant a project the status of European semiconductor technology initiative.

2. The Commission shall, taking into account the opinion of the European Semiconductor Board, assess the application through a fair and transparent process on the basis of all following elements:

   (a) compliance with the criteria set out in Article 14(2) and commitment to comply with the requirements set out in Article 14(6);

   (b) a business plan evaluating the financial and technical viability of the project, taking into account ~~its~~**the project's** entire lifetime, including information on any planned public support;

   (ba) a description of expected spillover effects as referred to in Article 14(6), point (a);

   (c) proven experience of the applicant **or, in the case of a consortium, of at least one participating entity,** in operating similar initiatives **of a comparable technical and operational nature**;

   (d) provision of an appropriate supporting document ~~proving~~**demonstrating** the readiness of the Member State or Member States where the applicant intends to establish its facility to support the establishment of such an initiative **or, where no public support is sought, an endorsement of the application by the Member State concerned**;

PUBLIC

(e) the existence of appropriate policies and appropriate licensing agreements, including technical protection and implementing measures, aiming to ensure the protection of undisclosed information and IP rights, in particular with a view to ~~preventing the unauthorised disclosure of~~**protecting** trade secrets ~~or the leakage of~~**and** sensitive emerging technologies.

The Commission shall provide guidance on the information required under the first subparagraph and its relevant format.

3. The Commission shall process applications, adopt its decisions and notify the applicants within three months of receipt of a complete application. Where the Commission considers that the information provided in the application is incomplete, it shall provide the applicant with the opportunity to submit the additional information required to complete the application without undue delay. The Commission's decision shall determine the duration of the status on the basis of the predicted lifetime of the project.

4. The Commission shall monitor the progress achieved in the establishment and operation of European semiconductor technology initiatives and shall inform the European Semiconductor Board on a regular basis**, including information on participation and geographical distribution across Member States**.

5. The operator of the initiative may request the Commission to review the duration of the status or to modify its implementation plans with regard to compliance with the requirements set out in Article 14(6) where ~~it~~**the operator** considers such a review to be duly justified on account of unforeseen external circumstances**, such as technological developments or changes in market demand**. On the basis of such a review, the Commission may revise the duration of the status granted in accordance with paragraph 3 of this Article or accept the modification of the implementation plans.

6. Where the Commission finds that an initiative no longer fulfils the requirements set out in Article 14(6), it shall give the operator of the European semiconductor technology initiative the opportunity to comment and to propose appropriate **corrective** measures.

PUBLIC

7. The Commission may repeal a decision recognising the status of a European semiconductor technology initiative if the recognition was based on an application containing incorrect information or where, despite completing the procedure in paragraph 5 of this Article, the European semiconductor technology initiative does not fulfil the requirements set out in Article 14(6). Before taking such a decision, the Commission shall consult the European Semiconductor Board after providing it with the reasons for the proposed repeal. Any decision repealing the status of a European semiconductor technology initiative shall be properly reasoned and subject to a right of appeal by the operator.

8. Initiatives whose status as European semiconductor technology initiative have been repealed pursuant to paragraph 7 of this Article shall lose all rights linked to the recognition of this status arising from this Regulation. However, such initiatives shall remain subject to the obligation set out in Article 42(1) for a period equivalent to that which was initially laid down when the status was granted in accordance with paragraph 3 of this Article, or, where the status was reviewed, the applicable duration in accordance with paragraph 5 of this Article.

Article 16

Strategic projects

1. The Commission**, taking into account the opinion of the European Semiconductor Board,** shall recognise as Strategic Projects ~~semiconductor~~**those** projects that meet all of the following requirements:

   (a) it provides significant added value to the Union by substantially contributing to **the** objectives of **this Regulation and thus to the** common Union interest;

   (b) ~~the strategic project~~**it** is carried out by domestic ~~undertakings~~**entities**;

   (c) ~~strategic projects shall~~**it** demonstrate that ~~they~~**it** will articulate ~~their~~**its** supply chain in a way that reduces supply chain dependence on non-domestic ~~undertakings~~**entities** and strengthen the Union's security of supply;

(d) it has a clear cross-border dimension, in particular through technical **or operational** cooperation or public support involving more than one Member State;

(e) it contributes to the **competitiveness, indispensability**, resilience and ~~robustness~~**prosperity** of the Union's semiconductor value chain;

(f) it contributes to strengthening the Union's technological sovereignty and technological leadership by enabling, advancing or securing critical capacities, technologies or capabilities within the Union, including by reducing strategic dependencies~~.~~**;**

(fa) it has appropriate policies and appropriate licensing agreements in place, including technical protection and implementing measures, to ensure the protection of undisclosed information and IP rights, in particular with a view to protecting trade secrets and sensitive emerging technologies.

(fb) it supports the Union's talent pipeline by developing and deploying specialised educational and skills training, such as in close cooperation with the competence centres and other relevant stakeholders.

2. Multi-site strategic projects shall be operated by a single consortium ~~and shall function~~**which may operate** as an integrated legal and technical entity.

3. Participation in strategic projects shall be limited to Union entities.

4. By way of derogation from paragraph 3, participation of legal entities established in third countries is allowed, provided that such participation is consistent with the conditions referred to in paragraph 1 and such participation shall be subject to the relevant security-related conditions of the applicable Union programmes.

PUBLIC

Article 17

Identification of priority areas for strategic projects

1. A technical description of priority areas for potential strategic projects in certain indicative technological areas is set out in Annex II. ~~In order to update the technological descriptions and indicative technological areas listed in Annex II to reflect technological change and market developments relevant to the semiconductor sector the Commission is empowered to adopt delegated acts in accordance with Article 55 to amend Annex II.~~

~~1~~**1a**. In order to strengthen Union sovereignty and ensure security of supply in ~~semiconductors~~**chips**, the Commission~~, in accordance with Article 17(1),~~ shall treat ~~a~~**any** strategic project for a Union-based open foundry for advanced semiconductor manufacturing with the highest priority**, with due regard to the advancement of other priority areas across the semiconductor value chain**.

~~2~~**1b**. The open foundry for advanced semiconductor manufacturing referred to in paragraph ~~1~~**1a** shall constitute a facility or coordinated network of multi-site facilities located within the territory of the Union, capable of manufacturing and packaging advanced semiconductor technologies in accordance with state-of-the-art industrial capabilities.

~~3~~**1c**. The open foundry for advanced semiconductor manufacturing shall take into account the requirements and objectives set out by potential offtakers as set out in Article 8.

2. The Commission shall decide, taking into account the opinion of the European Semiconductor Board, on the basis of the criteria set out in Article 16(1) and the indicative technological areas referred to in Annex II, on the priority areas for potential strategic projects.

2a. In order to update the technological descriptions and indicative technological areas listed in Annex II to reflect technological change and market developments relevant to the semiconductor sector the Commission is empowered to adopt delegated acts in accordance with Article 55 to amend Annex II.

PUBLIC

Article 18

Designation of strategic projects

1. The implementation of actions supporting potential strategic projects **in the priority areas set out in Annex II** shall be entrusted to the Chips Joint Undertaking and carried out through actions set out in its work programme. **Calls and evaluation procedures shall be open and transparent.**

2. The Commission~~, taking into account the opinion of the European Semiconductor Board~~ shall, by means of a decision, designate as strategic projects those proposals selected for funding by the Chips Joint Undertaking that comply with the criteria set out in Article 16(1) and that request to be designated as such.

3. Subject to the consent of the applicant or applicants, proposals not selected for funding by the Chips Joint Undertaking may also be designated as strategic projects when they meet the applicable evaluation requirements laid down in the call for proposals and comply with the criteria set out in Article 16(1). The possibility to obtain such designation shall be clearly indicated in the calls for proposals and related application procedures and should be requested by the project.

4. The Commission's decision shall indicate whether a strategic project qualifies as a first-of-a-kind initiative in accordance with this Regulation, and shall determine the duration of the status of first-of-a-kind on the basis of the predicted lifetime of the project.

5. ~~Projects designated as~~**In its decision designating** strategic projects **the Commission** shall ~~benefit~~**specify whether the strategic project complies with the requirements laid down in Article 14(6) and thus benefits** from the **same** rights and ~~be~~**are** subject to the **same** obligations applicable to European semiconductor technology initiatives under this Regulation ~~when they comply with the requirements laid down in Article 14(6)~~.

PUBLIC

6. The strategic project may request the Commission to review the duration of the status of strategic project or to modify the operator's implementation plans with regard to compliance with the requirements laid down in Article 16(1), where the operator considers such a review to be duly justified on account of unforeseen external circumstances**, such as technological developments or changes in market demand**. On the basis of such a review, the Commission may revise the duration of the status of strategic project granted or accept the modification of the implementation plans.

7. Without prejudice to any suspension or termination of funding agreements between the operator implementing the strategic project and the Chips Joint Undertaking, where the Commission finds that a project designated as a strategic project no longer fulfils the criteria laid down in Article 16, or where its designation was based on an application containing incorrect information affecting compliance with those criteria, it may, taking into account the opinion of the European Semiconductor Board, withdraw the designation of that project by means of a decision.

8. Before adopting a decision pursuant to paragraph ~~6~~**7** of this Article the Commission shall provide the operator implementing in the strategic project with the reasons for the envisaged withdrawal and shall give them the opportunity to submit observations **and propose corrective measures** within an appropriate time limit. The Commission shall take due account of those observations. Any decision withdrawing the status of strategic project shall be properly reasoned and subject to a right of appeal.

9. Projects for which the designation as a strategic project has been withdrawn shall lose all rights and obligations connected to the status of strategic project under this Regulation. However, such projects shall remain subject to the obligation set out in Article 43(1) for a period equivalent to that which was initially foreseen when the status was granted.

~~*Article 19*~~

~~**Advanced semiconductor manufacturing**~~

~~1. In order to strengthen Union sovereignty and ensure security of supply in semiconductors, the Commission, in accordance with Article 17(1), shall treat a strategic project for a Union-based open foundry for advanced semiconductor manufacturing with the highest priority.~~

~~2. The open foundry for advanced semiconductor manufacturing referred to in paragraph 1 shall constitute a facility or coordinated network of multi-site facilities located within the territory of the Union, capable of manufacturing and packaging advanced semiconductor technologies in accordance with state-of-the-art industrial capabilities.~~

~~3. The open foundry for advanced semiconductor manufacturing shall take into account the requirements and objectives set out by potential offtakers as set out in Article 8.~~

Article 20

Coordination of financing

1. The Commission may carry out activities, where appropriate in cooperation with Member States, to crowd-in investments for European semiconductor technology initiatives and strategic projects. Such activities may, without prejudice to Articles 107 and 108 TFEU, include providing and coordinating support to European semiconductor technology initiatives and strategic projects that face difficulties in accessing financing, in synergy with Union programmes **as referred to in Annex IV of this Regulation, with a view to ensuring complementarity between Union, national, regional and private financing and facilitating cross-border participation in relevant projects**.

2. The European Semiconductor Board ~~shall~~**may**, at the request **of a Member State on behalf** of a European semiconductor technology initiative or a strategic project, provide advice on the financing of the initiative or project, taking into account the funding already secured and considering at least the following elements:

   (a) additional public and private sources of financing, including equity **or any other financial instrument or support measure**;

   (b) support through resources from the European Investment Bank or other financial institutions;

   (c) existing Member State instruments and programmes, including from export credit agencies, national promotional banks and institutions;

   (d) relevant Union funding and financing programmes.

2a. **The Commission shall continue to promote activities to facilitate and accelerate access to Union funding as well as other funding, in particular for start-ups, scale-ups, SMEs and small mid-caps.**

SECTION 2

PERMIT-GRANTING PROCEDURES

Article 21

Fast-tracking of permit-granting procedures

1. Member States shall ensure that administrative applications related to the ~~planning,~~ construction ~~and~~**,** operation **and, where relevant, the planning stage of prospective**~~of~~ European semiconductor technology initiatives and strategic projects are processed in an efficient, transparent and timely manner.

2. The permit-granting procedure for **prospective** European semiconductor technology initiatives or strategic projects shall not exceed 12 months, from the ~~moment a complete~~**date of acknowledgement of the completeness of the** application ~~has been submitted to the one stop shop~~**by the single point of contact**.

2a. **In exceptional and duly justified cases, where the nature, complexity, location or size of the prospective European semiconductor technology initiative or strategic project so require, Member States may extend, before their expiry and on a case-by-case basis, the procedure by a maximum of six months.**

2b. **In the event of an extension referred to in paragraph 2b, the single point of contact concerned shall inform the applicant in writing of the reasons justifying the extension and of the deadline for the decision. In the case of a prospective strategic project which has been selected to receive Union funding it shall also notify the Commission.**

3. The time limit set in paragraph 2 shall be without prejudice to any shorter time limits set by Member States.

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4. Where such a status exists in national law, European semiconductor technology initiatives and strategic projects shall be allocated the status of highest national significance possible and be treated as such in permit-granting processes. This paragraph shall apply only where such status exists in national law and shall not create an obligation for Member States to introduce such status.

Article 22

~~One stop shop~~Single point of contact for permit-granting procedures

1. Member States shall designate ~~a one stop shop~~**one or more single points of contact** responsible for centralising and coordinating the application of European semiconductor technology initiatives and strategic projects under this Article.

1a. Where a Member State designates more than one single point of contact, it shall ensure that only one such single point of contact is responsible for a European semiconductor technology initiative or strategic project.

1b. A single point of contact shall act as a coordination and communication interface and shall not affect the allocation of decision-making powers under national law, unless a Member State decides otherwise.

2. Member States shall establish a ~~single~~ permit-granting procedure based on a single application to ~~the one stop shop designated pursuant to Article 22(1)~~**their single point of contact**, covering all permits required for European semiconductor technology initiatives and strategic projects.

~~3. The one stop shop shall serve as a single point of contact for the European semiconductor technology initiative or strategic project.~~

4. No later than 45 days from the receipt of ~~the single~~**an** application, the ~~designated one-stop-shop~~**single point of contact** shall acknowledge that the application is complete or request any missing information needed to process the application.

5. Where, after the submission of any missing information, ~~the~~**an** application is still deemed to be incomplete, the ~~one stop shop~~**single point of contact** may, within 30 days of the submission of the requested missing information, make a second request for any information still missing. The ~~one- stop- shop~~**single point of contact** shall not request information in areas not covered in the first request for additional information and shall request further information only as necessary to cover the missing information.

6. If the establishment of a European semiconductor technology initiative **or strategic project** requires decisions to be taken in two or more Member States, the relevant ~~one stop shops~~**single points of contact** shall take all necessary steps for efficient and effective cooperation and coordination among themselves.

Article 23

Facilitating administrative and permit-granting process

1. European semiconductor technology initiatives and strategic projects within the meaning of this Regulation shall be considered strategic projects contributing to resilience and decarbonisation or resource efficiency for the purposes of Article 14(1) of [Proposal for a Regulation on speeding-up environmental assessment]. Points 1, 2 and 3 of the Annex ~~in~~**to** that Regulation shall apply.

2. Without prejudice to [the Proposal for a Regulation on speeding-up environmental assessment], Member States shall ensure that any **relevant** studies carried out, or permits or authorisations issued, related to the ~~planning,~~ construction ~~and~~**,** operation **and, where relevant, planning stage** of European semiconductor technology initiatives and strategic projects are taken into account and that no duplicate studies, permits or authorisations are required, unless otherwise required under Union or national law.

PUBLIC

Article 24

~~Use of European Business Wallets by the~~ Single access portal

1. Member States shall set up**, or make available through existing structures, including those established by Member States or Union law**, a single access portal ~~at national level~~ for the submission of the single ~~permit~~ application **for permitting** for European semiconductor technology initiatives and strategic projects referred to in Article 22(2).

The single access portal shall automatically attribute the permit applications to the relevant authority, inform the applicant about all steps of the permit-granting procedure, the status of the procedure and of the decisions of authorities, and enable the applicant to check compliance with applicable deadlines.

2. The single access portal shall **enable the use of the core functionalities of**~~use~~ the European Business Wallets established pursuant to [Proposal for a Regulation on the establishment of European Business Wallets].

3. ~~Through the use of European Business Wallets,~~ The single access portal shall enable:

(a) interoperability and automated data exchange between relevant authorities;

(b) re-use of data and documents already held by relevant authorities;

(c) a high level of cybersecurity, and integrity of information;

(d) transparency and accountability of the permit-granting procedure.

4. When setting up single access portals, Member States shall, where appropriate, make use of existing Union digital infrastructure, catalogues and building blocks established by Union law.

5. The ~~designated one stop shop as~~**single points of contact** referred to in Article 22 ~~of this Regulation~~ shall have access to all relevant data and information available in the single access portal, in order to perform ~~its~~**their** duties.

Article 25

Online accessibility of information

1. Member States shall provide access to the following information on processes relevant to the development of potential European semiconductor technology initiatives and strategic projects, online and in ~~a centralised and~~**an** easily accessible manner:

   (a) the European Business Wallets referred to in Article ~~24~~**24(2)**;

   (b) the permit-granting procedure, including information on dispute settlement;

   (c) financing and investment services;

   (d) funding possibilities at Union or Member State level**, including, where relevant at regional level**;

   (e) business support services, including corporate tax declaration, local tax laws ~~or~~**,** labour law~~.~~ **and other relevant administrative requirements;**

   (ea) competence centres.

2. The Commission shall, in a centralised**, uniform** and easily accessible manner, refer to the information provided by the Member States on its website to ensure a comprehensive and clear overview of all relevant information per Member State.

PUBLIC

SECTION 3

EUROPEAN SEMICONDUCTOR REGIONS OF EXCELLENCE

Article 26

European Semiconductor Regions of Excellence label

1. The Commission may decide to award the European Semiconductor Region of Excellence label by means of **an** implementing act. The label may be awarded following an application by **one or more regional authorities from the same Member State or, in Member States with no regional level of administration, by the Member State. In the case the applicant is** a regional authority ~~and~~**the application** shall be explicitly endorsed by the relevant Member State.

2. ~~The~~**An** application **referred to in paragraph 1** shall ~~include~~**take the form of** a Semiconductor Region Investment Plan, ~~demonstrating a shared strategic vision by all relevant authorities~~**endorsed by the Member State concerned**.

3. Without prejudice to the applicable rules governing Union programmes and instruments **and in order to encourage the development of existing and emerging semiconductor ecosystems across the Union**, the European Semiconductor Regions of Excellence label may be ~~taken into account~~**considered** when assessing and selecting **relevant** operations proposed under Union funding programmes.

PUBLIC

Article 27

European Semiconductor Region Investment Plan

1. The European Semiconductor Region Investment Plan as referred to in Article 26(2) shall include a description of the region, including its geographic scope and~~, at least,~~ **the relevant elements from** the following ~~elements~~**list**:

   (a) strategic vision and scope:

      (i) assessment of the existing industrial and semiconductor ecosystem in the region, including existing ~~semiconductor~~**chip** manufacturing facilities; relevant end user sectors; its position in semiconductor value chains, with particular regard to its unique features and its potential contribution to the resilience and growth in the European semiconductor value chain;

      (ii) a strategic vision ~~for~~**outlining** the semiconductor-related development **potential** of the region over the next ten years, including, where relevant, the transformation or linkage of existing industrial activities towards ~~semiconductor-related~~**the semiconductor value chain and related** activities;

   (b) availability and further development of enabling conditions and infrastructure in the region concerned:

      (i) a description of measures to ensure access to sufficient, reliable and clean energy, including grid capacity and decarbonisation pathways in line with the European Climate's Law climate neutrality objective;

      (ii) a description of availability of suitable land and facilities for semiconductor value chain related activities, including zoning, land-use planning and industrial sites;

      (iii) a description of transport, communication networks and water infrastructure relevant to the semiconductor value chain related activities in the region;

      (iv) a description of **any** measures to ~~simplify and accelerate~~**support stakeholders in** permit-granting, licensing and administrative procedures~~, including the link with the one-stop-shop as referred to in Article 22~~;

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(c) support to innovation and research activities in the region concerned:

(i) a description of the research and innovation activities and their further support related to the semiconductor value chain in the region, including synergies with national and Union research and innovation programmes;

(ii) a description of cooperation with ~~universities,~~ research and ~~technology~~**knowledge-dissemination** organisations, including, where relevant links to the activities of pilot lines as referred to in Article 5, point (b) and ~~(~~**c) and** competence centres as referred to in Article 6;

(d) support to education, skills and workforce and its further development in the region concerned:

(i) a description of measures to ensure the availability of a skilled semiconductor-industry related workforce at all levels, with synergies of benefits provided under the Pact for Skills[36]**and other relevant initiatives**;

(ii) a description of partnerships between industry, education providers and public authorities in the area of semiconductors;

(iii) a description of actions to attract, retain and upskill semiconductor industry-related talent, including international talent where appropriate;

(e) support of industrial and investment attractiveness and its further development in the region concerned:

(i) a description of measures to attract and retain private investments relevant to the semiconductor value chain;

(ii) a description of measures to integrate ~~small and medium-sized enterprises~~**start-ups, scale-ups, SMEs** and small mid-caps into the regional ecosystem.

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36 Communication from the Commission to the European Parliament, the Council, the European Parliament, the European Economic and Social Committee and the Committee of the Regions, European Skills Agenda for sustainable competitiveness, social fairness and resilience, COM(2020) 274 final.

Article 28

Assessment of applications for the European Semiconductor Region of Excellence label

1. The Commission shall assess applications for the European Semiconductor Region of Excellence label **referred to in Article 26** on the basis of coherence and credibility of the Semiconductor Region Investment Plan and the level of commitment by the relevant authorities. **The assessment shall not be conditional on the existence of a developed semiconductor ecosystem.**

2. The Commission shall process applications, adopt its decision **by means of an implementing act as** referred to in Article 26(1) and notify the region, the Member State concerned and the European Semiconductor Board within three months of receipt of a complete application.

3. Where the Commission considers that the information provided in the application is incomplete, it shall inform the regional authority and Member State concerned without undue delay and provide the opportunity to submit the additional information required to complete the application.

4. The Commission's decision referred to in Article 26(1) shall determine the duration of the European Semiconductor Region of Excellence label, which shall be based on the assessment of the submitted Semiconductor Region Investment Plan.

5. The regional authority and the Member State concerned shall monitor the progress of implementation of the Semiconductor Region Investment Plan and shall ~~inform~~**update** the Commission and the European Semiconductor Board ~~at least~~ yearly. **The European Semiconductor Region of Excellence label may be subject to review by the Commission, following request from the regional authority or the Member State, if there is a substantial change in the circumstances underlying the designation.**

6. A summary of the Semiconductor Region Investment Plan, excluding commercially sensitive information and designed to attract investment, shall be made publicly available via both the following means:

   (a) a website of the Commission;

   (b) a website of the Member State, the region and/or relevant authorities concerned.

PUBLIC

Article 29

Network of European Semiconductor Regions of Excellence

1. A Network of European Semiconductor Regions of Excellence (~~'~~the **'**Network') shall be established.

2. The Network shall organise its work autonomously. It may establish its own working methods, including the organisation of meetings, the designation of a Chair on a rotating basis among participating regions, and the adoption of informal arrangements to facilitate cooperation and exchange of information.

3. The Network shall bring together regions that have been awarded the European Semiconductor Regions of Excellence label pursuant to Article 26.

4. The objectives of the Network shall include the following:

   (a) to facilitate cooperation and exchange of best practices among European Semiconductor Regions of Excellence **and, where relevant, with the European network of competence centres**;

   (b) to promote the Network and its activities among member and non-member regions through outreach, communication and dissemination activities to increase visibility and participation~~.~~**;**

   (c) to promote synergies and complementarities between regional semiconductor ecosystems across the Union, including **cross-border cooperation between regions and** across different segments of the semiconductor value chain **and with relevant stakeholders**;

   (d) to enhance the visibility and attractiveness of European Semiconductor Regions of Excellence for private investment ~~and~~ **,** international partnerships **and participation in relevant Union semiconductor initiatives**.

5. The Commission may facilitate the functioning of the Network and may organise meetings, workshops or other activities to support the exchange of information and cooperation among participating regions**, including the dissemination of best practices and lessons learned**.

SECTION 4

RESILIENCE IN SUPPLY CHAINS

Article 30

Public procurement

1. For procurement procedures falling within the scope of **[**Directives 2024/23/EU, 2014/24/EU or 2014/25/EU**]** and launched on or after [OJ: insert date one year after entry into force] concerning infrastructures, equipment or systems in sectors of high criticality, as listed in Annex I of Directive (EU) 2022/2555, and in other critical sectors, as listed in Annex II of that Directive, contracting authorities and contracting entities may require economic operators to submit, together with their tender documents, a security of supply declaration relating to the sourcing of ~~semiconductors~~**chips** incorporated into the infrastructures, equipment or systems covered by the contract.

2. **Where** the declaration referred to in paragraph 1 **is required by the contracting authority or contracting entity, they** shall **specify its required content. The requested information shall at least** include the following elements:

   (a) an overview of ~~undertakings~~**entities** involved in the supply of the ~~semiconductors~~**chips** incorporated in the ~~product~~**infrastructures, equipment or systems**, including the proportion of domestic ~~undertakings~~**entities**;

   (b) the Union added value, demonstrated by the contribution of the tender to reinforcing the European semiconductor supply chain, such as the inclusion of ~~first-of-a-kind~~**European semiconductor technology** initiatives and strategic projects as suppliers;

   (c) the semiconductor supply chain resilience and diversification strategy of the tenderer, such as the tenderer's dual sourcing strategy, including, where feasible and appropriate, the inclusion of at least one domestic ~~undertaking~~**entity, and contingency arrangements**;

   (d) where applicable, any recommendations or obligations referred to in Article 31;

(e) where applicable, the security of supply risk assessment performed in accordance with Article 32.

3. Where ~~a security of supply~~**the** declaration **referred to in paragraph 1** is required ~~from economic operators,~~**by the** contracting ~~authorities and~~**authority or** contracting ~~entities~~**entity, they** may specify, in the procurement documents, requirements relating to security of supply relating to the sourcing of ~~semiconductors~~**chips** incorporated into the infrastructures, equipment or systems covered by the public procurement contract. To that end, contracting authorities and contracting entities may include technical specifications, selection criteria, award criteria or contract performance clauses.

4. Requirements taken under paragraph 3 shall ~~be~~:

(a) **be** linked to the subject matter of the contract;

(b) not ~~conferring~~**confer** unrestricted freedom of choice on the contracting authority or contracting entity;

(c) ~~expressly set out in the procurement documents or in the contract notice;~~

(d) **be** ancillary and non-decisive in the award of the contract;

(e) **be** designed in line with the Union's international commitments.

5. Contracting authorities and contracting entities shall notify their national competent authority pursuant to Article 48 ~~of this Regulation~~ with the list of domestic ~~undertakings~~**entities** identified in the security of supply declarations issued by the economic operators**, subject to applicable confidentiality and proportionality requirements**.

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6. The national competent authority pursuant to Article 48 **shall compile, where necessary for the objectives** of this Regulation ~~shall compile a verified~~, **a** list of ~~all the~~ domestic ~~undertakings~~**entities** identified in public procurement procedures within the Member State. ~~The~~**Such** lists **shall not require the establishment or maintenance of a permanent register and** may be exchanged ~~partially or in full~~ between Member States ~~following the~~**only to the extent** necessary **and proportionate for the implementation of this Regulation and subject to the applicable** confidentiality requirements~~, pursuant to Article 50~~.

Article 31

Further actions on public procurement

1. Where the Commission identifies a ~~potential~~ supply chain risk in the context of the monitoring carried out pursuant to Article 35, it may, after consulting the European Semiconductor Board, issue recommendations to contracting authorities and contracting entities regarding the supply of ~~semiconductors~~**chips** by domestic ~~undertakings~~**entities** for procurement procedures referred to in Article 30(1)**, taking into account the specific characteristics of the sectors concerned and the availability of alternative sources of supply**.

2. Where the Commission establishes that the supply chain risks as identified in paragraph 1 persist, it may, ~~after consulting~~**taking into account the opinion of** the European Semiconductor Board and with regard to the principles of necessity and proportionality, adopt an implementing ~~decision~~**act** specifying for which specific infrastructures, equipment or systems as referred to in Article 30 contracting authorities and entities shall require a security of supply declaration from economic operators.

3. Contracting authorities and contracting entities may decide not to apply the requirements foreseen by the implementing ~~decision~~**act** referred to in paragraph 2 of this Article where one of the following conditions is fulfilled:

   (a) the required products or services can be supplied only by specific economic operators, and no reasonable alternative or substitute exists, and the absence of competition is not the result of an artificial narrowing down of the parameters of the procurement procedure;

(b) no suitable tenders or no suitable requests to participate were submitted, including in response to a similar former procurement procedure launched by the same contracting authority or contracting entity in the two years preceding the ~~start~~**commencement** of the planned new procurement procedure;

(c) taking the elements declared in accordance with Article ~~31~~**30**, paragraph 2~~, point (d)~~ into account would require a contracting authority or contracting entity to acquire goods, services or works having disproportionate costs or would result in technical incompatibility in their operation and maintenance.

~~(d) For the purposes of point (c), estimated cost differences exceeding 25% of the value of the tender, based on objective and transparent data, may be presumed by contracting authorities and contracting entities to be disproportionate;~~

(da) the contract in question is to be awarded in a procedure without prior publication because it is strictly necessary for reasons of extreme urgency brought about by events unforeseeable by the contracting authority or contracting entity and the time limits for the open or restricted procedures or competitive procedures with negotiation cannot be complied with;

~~(d)~~**3.** For the purposes of point (c), estimated cost differences exceeding 25% of the value of the tender**, project or contract**, based on objective and transparent data, may be presumed by contracting authorities and contracting entities to be disproportionate;

Article 32

Risk-prone sectors

1. After consultation ~~of~~**with** the European Semiconductor Board, and based on evidence of supply chain risks, the Commission may identify one or more sectors listed in Annex V or Annex VI, or their subsectors, as risk-prone by means of an implementing decision.

2. **Economic operators within sectors identified as risk-prone may carry out security of supply risk assessments.** The Commission may issue methodological guidance on how to carry out ~~security of supply risk~~**such** assessments and recommend possible mitigation measures for those sectors identified as risk-prone. This guidance shall address the following elements:

(a) dual sourcing strategy~~, including from at least one domestic undertaking~~;

(b) upstream and downstream supply chain mapping;

(c) vulnerability analysis and sensitivity to supply disruption.

3. ~~The~~**Information arising from a** security of supply risk ~~assessments~~**assessment** referred to in paragraph 2 of this Article may be **reused in the security of supply declaration** requested by contracting authorities or contracting entities in procurement procedures as referred to in Article 30(1) **and, where applicable, Article 31(2)**.

4. If, after consultation with the European Semiconductor Board, the Commission concludes that the recommended mitigation measures as referred to in paragraph 2 and which are necessary to ensure security of supply of ~~semiconductors~~**chips** or products integrating ~~semiconductors~~**chips** are not adequately taken over by the sector identified as risk-prone, it may adopt an implementing act on specific risk mitigation measures**. The implementing act shall specify the period of application of the risk mitigation measures** that sectors or subsectors shall take for specified ~~semiconductor~~**chip** products, namely mitigation measures related to:

(a) performance of a risk assessment;

(b) procurement of ~~semiconductors~~**chips**;

(c) dual sourcing**, including from at least one domestic entity where technically equivalent alternative suppliers exist and diversification is technically feasible**;

(ca) qualification of alternative suppliers;

(d) stockpiling**, where appropriate and proportionate to the identified risk**;

(e) diversification of supply of ~~semiconductors~~**chips** or related components.

5. After adoption of an implementing act **referred to** in ~~accordance with~~ paragraph 4, the Commission, based on evidence ~~of~~**that** the identified supply chain risks ~~having~~**have** been addressed and after consultation of the European Semiconductor Board, may revoke the risk-prone designation.

6. The Commission shall base its assessments carried out in accordance with this Article on evidence, including publicly available information, information gathered **in the context of the monitoring carried out pursuant to Article 35 and** through requests for information pursuant to Article 38, or the existence of repeated supply chain disruptions.

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ANNEX I

Actions under the Chips for Europe Initiative 2.0

Actions under this Annex shall be implemented with a view to ensuring open, transparent and non-discriminatory access across the Union, effective participation of start-ups and SMEs, and broad geographical reach, including for actors established in Member States that do not host the relevant infrastructure.

Technical description of the Chips for Europe Initiative 2.0: scope of actions

Where appropriate, the actions supported by the Chips for Europe Initiative 2.0 shall be implemented in accordance with the following technical descriptions:

1. Design capacities for integrated ~~semiconductor~~**chip** technologies

Context

The Chips for Europe Initiative 2.0 shall support large-scale innovative design capacities for ~~semiconductor~~**chip** technologies through a cloud-based design platform available across the Union. The design platform shall consist of innovative design facilities with extended libraries and tools, integrating a large number of existing and new technologies, including emerging technologies such as integrated photonics, quantum, and AI/neuromorphic. In combination with existing Electronic Design Automation tools, it shall allow the design of innovative components and new system concepts, and it demonstrates key functionalities, such as new approaches to high-performance, low-energy, security, new 3D and heterogeneous system architectures.

As the strategic backbone of the Chips for Europe Initiative 2.0, the platform shall provide a one-stop entry point, guiding users from design to prototyping and manufacturing, and uniting research, education, and industry. Its ultimate goal shall be to foster a new generation of Union fabless start-ups. Those companies contribute to developing innovative chips for Union user industries, capture the highest value in the semiconductor value chain, drive innovation in fast-growing markets, and reduce the Union's dependence on foreign design ecosystems.

Status

As of May 2026, a wide range of actors has been involved, including a Platform Coordination Team (PCT)[1], Design Enablement Teams[2], cloud providers, Electronic Design Automation (EDA) vendors, and IP providers. The design platform shall be implemented in a sequential manner: a Platform Coordination Team was first selected and put in place to operate the platform, host the central cloud infrastructure and coordinate user support services. The Design Enablement Teams have also been selected to provide tailored, end-to-end support for users throughout the chip development process. A contractor was selected for the central cloud infrastructure, which will host IP, pilot line Process Design Kits, and open-source EDA tools.

Negotiations are ongoing to select and onboard major EDA tool providers. These negotiations are expected to be concluded by autumn 2026. The first full-scale facilities are expected to become operational by end 2026.

The Design Platform shall be complemented by other actions to cultivate design related competences in the Union. This includes administering grants for start-ups and SMEs using the platform, support for open-source EDA tools development, and for the EuroPractice services that provide over 600 European universities with access to EDA tools for training at nominal costs as well as access to fabrication from leading foundries.

Future outlook

The Design Platform shall be continuously upgraded with new design capabilities as it continuously integrates more and more technologies and designs. This may include new open-source processor architectures and other innovative architectures, chiplets, programmable chips, new types of memory, processors, accelerators or low power chips.

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1 The Platform Coordination Teams serves as the hosting entity for the Design Platform's virtual infrastructure and central services, coordinates access to a wide range of tools, assets and services, and assists the Chips JU in procuring the cloud platform.

2 Design enablement teams assist users in setting up and customising design environments and flows, and to deploy Electronic Design Automation tools on the cloud.

The platform shall also integrate photonics and quantum chips IP, libraries and design automation tools in a fully integrated system approach (see also points 3 and 5 below). It shall also integrate the Process Design Kits (PDKs) of the main pilot lines of the Chips for Europe Initiative 2.0, as well as PDKs of industrial manufacturing facilities (subject to their prior agreement) in order to facilitate designing chips ready to be taped out in such pilot lines and industrial facilities.

The platform shall offer its services via the cloud, maximising access and openness to the whole community by networking existing and new design centres across the Member States. In particular, the platform shall offer support to startups, scaleups, and SMEs. It shall enlarge the Union's semiconductor ecosystem by integrating with different market sectors, such as health, mobility, energy, telecommunications, security, defence and space. More attention shall be given to industrialisation of innovative components designed on the platform and introduced on lead sectors.

2. Pilot lines for preparing for innovative production, testing and validation

Context

The Chips for Europe Initiative 2.0 shall support pilot lines for production, testing and validation bridging the gap from the lab to the fab of advanced ~~semiconductor~~**chip** technologies, such as architectures and materials for power electronics, neuromorphic and embedded AI chips, integrated photonics, graphene and other 2D-material-based technologies, integrating electronics and microfluidics in heterogeneous systems. **Access to pilot lines should contribute to the development of the entire semiconductor value chain.**

Status

As of May 2026, five pilot lines are operational to varying extents, while more equipment, machinery, and tools are being added to increase the capability and capacity of the pilot lines. The pilot line technology areas were chosen to close the Union's most critical semiconductor gaps while building on existing strengths, securing long-term competitiveness, security of supply, and industrial resilience. The five pilot lines are the following:

- sub-2 nm logic anchors the Union in the advanced nodes that power AI, HPC, data centres and next-generation communications;

- FD-SOI capitalises on a field where the Union already leads, delivering low-power, high-reliability chips for automotive, mobility, industrial automation, and Internet of Things;

- advanced packaging and heterogeneous integration follow the observation that future performance gains hinge on system-level integration; the Union faces a strategic weakness in packaging but also a major opportunity to lead in chiplets, 3D stacking, and the co-integration of logic, memory, sensing, and connectivity;

- wide-bandgap materials (such as SiC and GaN) match the Union's strengths in power electronics and are vital for the energy transition, electric mobility, renewable infrastructure, and high-efficiency industrial systems; and

- photonic integrated circuits, which are increasingly important for high-bandwidth, low-power data transmission, sensing and advanced computing architectures in telecoms and data centres.

Moreover, 'Lab to Fab Accelerators' aim to achieve a rapid uptake by EU industry of the technologies developed under the pilot lines, in particular technologies related to advanced packaging and heterogeneous integration. **These activities should facilitate technology transfer and industrial deployment across the entire European semiconductor ecosystem.**

Future outlook

Pilot lines shall continue to support experimentation, test, and validation, including through Process Design Kits (PDKs), of the performance of IP blocks, virtual prototypes, new designs and novel integrated heterogeneous systems in an open and accessible way. Their PDKs shall be integrated in the design platform in order to enable access for design and (virtual) prototyping projects.

Current pilot lines shall increasingly focus on industrialisation and deployment of pilot line technologies to support the Union's semiconductor ecosystem.

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New or upgraded pilot lines may be supported for emerging challenges, such as energy efficient AI chips; leading edge technologies such as CFET devices and monolithic 3D integrated circuits for higher performance and lower power consumption; ferroelectric, resistive and charge based memories enabling ultra-fast and ultra-low power operations**; and cutting-edge application-oriented pilot lines focused on first industrial deployment for critical sectors**. **Consideration should also be given to emerging opportunities across the value chain.**

Furthermore, new or upgraded pilot testbeds may be supported where different innovative technologies or products are combined and integrated for the development and validation of new devices in key applications and user industries. An example is a testbed for the miniaturisation, advanced optics, and laser projection technologies related to smart glasses. Pilot testbeds shall help identify risks, validate performance, and ensure feasibility in real-world conditions before full industrial-scale deployment. **Such testbeds should facilitate collaboration between industry, research organisations, competence centres and end-users.**

3. Advanced technology and engineering capacities for quantum chips

Context

The Chips for Europe Initiative 2.0 shall support the development of quantum chips and associated technologies, including those based on semiconductor material or integrated with photonics. Dedicated actions shall include design libraries for quantum chips, pilot lines for building quantum chips, and facilities for testing and validating quantum chips produced by the pilot lines. The aim is to provide Union researchers, start-ups and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies.

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Status

As of May 2026, six quantum chip pilot lines are established, one for each of the leading Union technology platforms: superconducting, spin, photonic, diamond, neutral-atom, and trapped-ion chips. The projects focus on setting up stable pilot-scale fabrication processes, integrating testing and experimentation facilities, developing early industrialisation roadmaps, and laying the groundwork for future scaling.

Pilot line	Name	Coordinator
Superconducting	SUPREME	VTT (FI)
Spin	SPINS	IMEC (BE)
Photonic	P4Q	University of Twente (NL)
Diamond	DIREQT	CNR (IT)
Neutral atoms	Q-PLANET	PASCAL (FR)
Trapped ion	CHAMP-ION	SAL (AT)

In addition, activities shall be addressed to support the emergence of a pan-European quantum design community around quantum chip design, simulation, and verification libraries and tools. Finally, enabling technologies shall be supported, including the electronics, cryogenics, packaging and interfacing subsystems that prepare, protect, control, interconnect, and read-out core quantum devices.

Future outlook

Advanced technology and engineering capacities for quantum chips shall continue to be built out and enhanced. This includes design capabilities, design libraries for quantum chips, pilot lines, testing and experimentation facilities, enabling technologies. Support to first industrialisation efforts of the most mature developments shall also be provided. A differentiation in support shall be made for different technology platforms. Maturation of quantum chip technologies shall lead to increased industrialisation. **Open access to relevant infrastructures and facilities should continue to be promoted where appropriate and under fair and transparent conditions.**

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4. A network of semiconductor competence centres and skills development

Context

The Chips for Europe Initiative 2.0 shall support the operation of a network of semiconductor competence centres. These centres shall provide structured access to technical expertise, testing facilities, and advisory services, and enable companies (particularly SMEs and start-ups) to strengthen their design capabilities, experiment with new technologies, and develop specialised skills. Competence centres shall play a key role in addressing the Union's skills gap in ~~semiconductor~~**chip** technologies.

Status

As of May 2026, competence centres have been established in all Member States, as well as in Norway. In addition, a support action was defined to set up and coordinate the work of the national competence centres. The support action has launched a Training and Skills Development focus group which drives collaboration among the competence centres to roll out education and upskilling initiatives, to create training concepts, and to provide specific training and access to the design platform and pilot lines.

Future outlook

Semiconductor competence centres shall continue to be supported. The possibility to launch new centres or to refocus existing centres depending on market and technology developments shall be analysed. The cooperation between competence centres in the overall network shall be strengthened, where possible. Furthermore, the support by competence centres on skills development shall be enhanced, including by fostering cooperation with higher education and vocational training providers, by collaborating closely with the Pact for Skills and the skills working group of the Industrial Alliance, and by increasing the visibility and attractiveness of the semiconductor sector. **Competence centres should also support technology transfer, industrial uptake of research results and integration of national ecosystems into European semiconductor value chains.**

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5. Advanced design, prototyping, and industrial deployment capacities for photonic integrated circuit technologies

Context

This new component of the Chips for Europe Initiative supports the development of photonic integrated circuits and associated technologies. Actions include developing design libraries and design automation tools for photonic integrated circuits and enhancing existing and/or setting up new pilot lines for the prototyping and production of photonic integrated circuits. Capabilities in production technologies including co-packaging and heterogeneous integration with electronic chips, manufacturing equipment, and materials platforms for photonic integrated circuits shall be strengthened. **Testing, validation and advanced photonic packaging capabilities should also be supported where appropriate.**

Status

As of May 2026, a pilot line on photonic integrated circuits has been inaugurated. This pilot line offers open-access fabrication services across 14 hosting sites, covering multiple photonic material platforms from silicon and silicon nitride to indium phosphide. Services include chip fabrication runs, hybrid integration, packaging, testing, and reliability qualification. Technology demonstrators are planned, including co-packaged optics for AI data centres, LiDAR sensors, visible light engines for AR/VR, and programmable photonic processors. Furthermore, apart from the pilot line, industrial-grade demonstrators of advanced photonic technologies are developed that need to show scalability, reliability, and integration-readiness. **Broad participation by companies, research organisations and competence centres from across the Union should be encouraged.**

Future outlook

Photonic integrated circuits and associated technologies shall continue to be supported. This shall include design tools, design libraries, pilot lines, demonstrators, training services. Specific attention shall be dedicated to the transfer and industrial uptake of technologies developed under this component of the Chips for Europe Initiative 2.0.

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6. Chips Fund activities for access to capital by start-ups, scale-ups, ~~and~~ SMEs **and small mid-caps**

Context

The Chips for Europe Initiative 2.0 shall support the creation of a thriving ~~semiconductor and quantum~~**chip** innovation ecosystem by supporting access to venture capital for start-ups, scale-ups and SMEs to grow their business and expand their market presence in a sustainable manner. **Such support should be available to innovative actors across the semiconductor value chain.**

Status

As of May 2026, the Chips Fund is implemented through two thematic investment facilities: the European Innovation Council's Accelerator programme, with Horizon Europe funding in blended grant and equity for high-risk, deep-tech startups; and the InvestEU Fund, managed by the European Investment Fund, with a guarantee from the Digital Europe Programme, for intermediated equity investments ranging from seed to growth stage. The EUR 300 million available budget for the Accelerator programme was fully deployed in just two years and supports 24 highly innovative startups with a total of EUR 62 million in grants and EUR 238 million in recommended equity investment. On the InvestEU leg of the Chips Fund, four financial partners have been selected and EUR 68 million in funds have been signed or approved with them, resulting so far in 31 companies from early to growth stage having received EUR 116 million equity investment.

Future outlook

Whereas attention for startups shall continue, more focus shall be put on scaleups and later stage funding. Considerable funding from the Scaleup Europe Fund for deep-tech scaleups shall be increasingly deployed, leveraging additional private venture capital. **The 'Chips Fund', in cooperation with similar instruments from Member States, should complement, though not exclusively, the transfer and industrial uptake of technologies developed under Operational Objectives 1 to 5.**
Industrialisation of pilot-lines technologies is a clear example to coordinate instruments from different institutions to enhance and accelerate its market uptake

PUBLIC

7. Grand challenges

Context

This new component of the Chips for Europe Initiative 2.0 shall support large-scale, cross-sectoral initiatives addressing major technological and industrial challenges of strategic relevance for the Union ('grand challenges'), which potentially affect different ecosystems. Grand challenges are expected to result in technology advances in mainstream and leading-edge technologies, end-to-end product integration through the whole product development lifecycle, and their pre-commercial industrialisation.

Status

As of May 2026, no prior activities have been carried out under the banner of 'grand challenges' under the Initiative.

Future outlook

Possible grand challenges that can be targeted may include the development of new computing technologies for drastic (say times 1000) energy reduction. The grand challenge would result in energy-efficient, secure and distributed AI infrastructures, enabling high-performance AI accelerators (HBM-class memory, stacked logic, optical/RF interconnects), agentic/embodied AI systems, contextual edge intelligence and secure low-power infrastructures. The development of energy-efficient chips, including AI chips, shall also support the grand challenge "pioneering energy- and resource-efficient compute infrastructure, with a view to enhancing their sustainability at scale" as identified under the Cloud and AI Development Act (CADA)[3]. A close link between the R&I activities to address the two complementary challenges shall be established, including possible coordinated calls for proposals. **Participation from research and knowledge-dissemination organisations, industry and innovative SMEs should be encouraged where appropriate.**

[3] See Article 4 of the Cloud and AI Development Act

Another grand challenge shall be the development of processors and accelerators, which are designed and, where appropriate, manufactured in the EU, and that would become part of a cloud and AI stack. This grand challenge shall again be closely linked and contribute to a CADA grand challenge, namely 'reaching autonomy across the cloud and AI stack, with a view to eliminate dependencies in critical technologies' [4]. The grand challenge may target in particular solutions developed by upcoming startups and may include the use of innovation procurement. Again, a close link between the R&I activities to address the two complementary challenges shall be established, including possible coordinated calls for proposals.

A third grand challenge may be in physical AI, to provide the foundational technologies to enable a wide range of future applications, services, and autonomous systems from, for example, humanoid to industrial robots and their deployment, in particular, in med-tech and healthcare to manufacturing, aerospace and defence. R&I in physical AI shall lead to advances in mainstream technologies such as power semiconductors, microcontrollers, and analog-/mixed signal- and sensor technologies. R&I shall be followed by industrial production and commercialisation of embedded advanced AI into autonomous machines, robots, broadband networks, and next-generation connected devices. **The activities should support collaboration across the semiconductor value chain.**

A fourth grand challenge may be on smart glasses and virtual worlds. A recent Commission Communication sets out the strategy and proposed actions on virtual worlds and Web 4.0[5]. In this context, optics, photonics and semiconductor technologies are crucial for realizing sensing and visualization devices supporting Virtual Worlds applications such as smart glasses. R&I shall significantly improve the quality, performance, and efficiency of processing and communicating Virtual Worlds content. A grand challenge for smart glasses shall aim at integrating relevant ultra-low power components, such as power electronics, sensors, cameras, audio devices, lasers, specialty glasses, displays, neuromorphic or AI chips into working prototypes and demonstrators.

Grand challenges may address market targets as well, for example, taping out chips from 100 fabless startups including 10 unicorns by 2035. Another type of grand challenges may address lead

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4 See Article 5 of the Cloud and AI Development Act

5 Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, "An EU initiative on Web 4.0 and virtual worlds: a head start in the next technological", COM(2023) 442 final, 11 July 2023.

markets and demand stimulation, for example, by developing automotive hardware platforms or the full stack for AI (Giga) Factories. Grand challenges may also address new semiconductor production technologies, for instance increasing recycling and boosting circularity of materials, or the development of advanced ~~semiconductors~~**chip** cooling technologies. **They should also support the participation of innovative start-ups, scale-ups, SMEs and research and knowledge-dissemination organisations across the Union.**

Industrialisation of new technologies shall be an essential part of the grand challenges.

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Annex II

Priority areas for strategic projects

Technical description of potential priority areas for strategic projects: scope of actions

1. European Advanced Semiconductor Manufacturing[1]

Reinforced action should be taken to create a sustained demand for advanced ~~semiconductors~~**chips** through the development of the EU advanced technology ecosystem. EU sovereignty and supply security in the area of advanced chips production and innovation is essential to foster a thriving and competitive EU semiconductor ecosystem, with reduced reliance on foreign supply chains. This is particularly important to cater for the increased demand for AI and cloud infrastructure. In addition, advanced chips are indispensable for strategic industry sectors such as defence, health, space, robotics, healthcare, secure communications, drones, and autonomous vehicles. They are also critical inputs for emerging and high-value areas such as photonics and quantum chips.

This strategic project aims to establish an EU semiconductor plant that combines leading-edge node chip manufacturing with chiplet integration and 2.5D/3D packaging. It shall build on solid research foundations, which have been validated in the Chips for Europe Initiative under the Chips Act. The manufacturing facility shall adhere to European values, including guarantees for confidentiality, integrity and traceability of chips, in particular for sensitive and strategic applications and infrastructure. European companies could help create demand by offering growth incentives for fabless chips and AI-driven system design. Public and private investments are estimated between EUR 20 and 40 billion depending on the option chosen. EUR 3 to 4 billion public and private investments could be mobilised to foster the growth of fabless chip design companies across the EU through funding from under the next MFF, Member States, and relevant industries and private investors.

[1] This part expands on a potential implementation of Article 19.

This project to be developed in close collaboration with domestic and international stakeholders, including credible technology and manufacturing partners, shall enable the establishment of cutting-edge capacities that reduce structural dependencies on non-EU suppliers, increase supply security for sectors such as AI, defence, space, healthcare, telecoms and automotive, and reinforce the EU's technological sovereignty.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

2. AI chips and systems for EU compute infrastructure

The Union is currently dependent on foreign AI chips and integrated systems, resulting in significant capital outflow to import critical foreign AI technologies. Strengthening the Union's technological sovereignty therefore requires building competitive, home-grown capacity at chip level and across the entire compute stack.

This strategic project aims to design, develop, prototype, and tape-out AI chips and compute systems based on advanced European technologies. AI chip design shall result in the development of demonstrators and prototypes that can be evaluated on a common testbed against clear benchmarks. Full-rack AI system prototypes shall be developed, including AI accelerators, high bandwidth memory, boards, ultra-low-latency networking and full software stack, and shall be delivered for comparative evaluation on agreed workloads. Rack-level system prototypes shall be demonstrated on a common EU testbed. Final testing and scoring shall use clear KPIs on common EU testbeds operated by a neutral facility.

This strategic project shall reduce reliance on non-EU suppliers and increase technological sovereignty across the full AI stack. It shall strengthen the EU ecosystem for design, integration and optimisation of high-performance AI systems, with R&D activities, data handling and testing executed in the Union, thereby anchoring skills, know-how and supply chains in Europe. Take-up of the AI systems shall create further demand to justify further investments in manufacturing in Europe.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

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3. Automotive application processor for autonomous driving

The automotive industry is currently undergoing a pivotal transformation, primarily driven by the emergence of electric, connected, autonomous vehicles. This shift necessitates a more centralised, integrated, and flexible electrical/electronic (E/E) architecture to accommodate the advanced computing needs of autonomous driving systems, ensure seamless vehicle connectivity, support electric vehicle (EV) power management, and enable new mobility services. Currently, European automotive OEMs rely on non-European suppliers for the application processors that enable autonomous driving, which creates dependencies, possible vulnerabilities that can be exploited, as well as potential security risks.

This strategic project aims to design, develop, prototype, and tape-out high-performance RISC-V based automotive application processors. These processors shall include advanced computer architecture techniques, multi-core configurations and support for high-bandwidth memory interfaces, catering to the complex computing demands of autonomous driving systems. In addition, AI and ML accelerators shall be developed with specialised Instruction Set Architecture (ISA) extensions for efficient data-intensive computations. These accelerators shall be optimised for automotive applications, supporting advanced AI models with a focus on energy efficiency, reduced latency, and real-time processing capabilities. The end result shall be an industry-grade silicon tape-out, incorporating a competitive RISC-V application processor alongside memory, accelerators and any other relevant IP taking advantage of advanced packaging techniques. A mature toolset shall accompany the hardware development. Automotive companies shall be able to deploy the results in an operational environment as qualified devices.

The strategic project shall address Europe’s technological sovereignty in automotive AI processors and accelerators. It shall reduce the dependence of European automotive OEMs on foreign suppliers. Take-up of the application processors and accelerators shall create further demand to justify further investments in manufacturing in Europe. **The project should also contribute to strengthening European capabilities in semiconductor design, advanced packaging and related enabling technologies.**

PUBLIC

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

4. ~~European~~**Innovative** memory ~~fabrication facilitys~~**tacks**

Memory chips, such as DRAM, NAND, and emerging non-volatile memories, are essential components in datacentres, AI systems, automotive electronics, telecommunications equipment, industrial automation, and defence applications. Currently, the global memory market is heavily concentrated in Asia (South Korea, Taiwan, China) and the United States. The EU lacks indigenous memory production capacity, leaving critical European supply chains highly vulnerable to geopolitical shocks, trade disputes and natural disasters. This dependency has become critically apparent in 2026, as surging demand for AI-related high-bandwidth memory (HBM) has led manufacturers to reallocate production capacity away from standard DRAM and NAND, triggering price surges in some segments and severe allocation shortages for European industries. Hence, the absence of a European memory fab constitutes a strategic vulnerability for the EU's digital sovereignty, economic resilience and defence readiness. A strategic project for a European memory fab would be necessary not only to secure supply for key industries, but also to anchor advanced manufacturing know-how, stimulate innovation across the semiconductor value chain and support the EU's broader objectives under industrial, digital, and economic security policies.

The strategic project for the establishment of a European memory fabrication facility shall require a consortium-based approach, combining public funding from the EU and participating Member States with substantial private investment, likely in the range of EUR 15-30 billion given the capital intensity of modern memory fabs. A European-led joint venture could be considered to build a differentiated position, such as embedded memory, low-power memory, or emerging technologies linked to AI and edge computing. A phased approach may begin with a pilot/R&D line before scaling to high-volume manufacturing, mitigating risk and building capability incrementally.

PUBLIC

A dedicated call for expressions of interest may be structured to identify industrial partners, technology providers, and Member State hosts willing to commit to this strategic initiative. **The proposals should take into account their contribution to the resilience, technological sovereignty and competitiveness of the Union and their ability to create positive spill-over effects across the European semiconductor ecosystem.**

5. Leading-edge chip design

While building physical manufacturing facilities is vital, a large share of the economic value, profit margins, and technological control in the semiconductor supply chain lies in chip design, architecture, and intellectual property. Europe has important strengths in research, automotive semiconductors, and semiconductor equipment; however, it remains comparatively weak in the large-scale design of the most advanced logic chips, particularly those based on leading-edge architectures and process nodes. As a result, the EU relies heavily on non-European companies for advanced compute and AI capabilities. **Semiconductor design should therefore be recognised as a strategic capability in its own right within the European semiconductor ecosystem.**
Without indigenous leading-edge design capacity, Europe risks remaining dependent on foreign architectures, leaving critical infrastructure, defence, and AI-related industries exposed to geopolitical restrictions, supply dependencies, and vendor lock-in. Strengthening chip design capabilities would allow the EU not only to capture more value within the semiconductor value chain, but also to embed European priorities such as security, privacy, resilience, and energy efficiency directly into advanced hardware.

A strategic project for ~~leading-edge~~**innovative** chip design shall aim to establish ~~sovereign,~~ world-class capability within the EU for the design of cutting-edge logic chips **memory and new functionalities**, focusing on intellectual property, architecture, and verification rather than manufacturing. Focus areas may include:

- Advanced AI accelerators for cloud, edge, and industrial applications (including for geospatial modelling and digital twins)**, while also supporting specialised industrial and scientific application domains relevant for European competitiveness**

- High-performance processors for supercomputing and datacentres

- Secure-by-design chips for critical infrastructure, defence, aeronautics and space
- Domain-specific processors for autonomous vehicles, robotics, and industrial automation
- Application-Specific Integrated Circuits (ASICs) and System-on-Chips (SoCs) for 5G/6G telecommunications **and other strategic industrial applications**
- RISC-V-based open-architecture processors at leading-edge nodes
- Advanced chiplet platforms for 2.5D/3D integration across automotive, aerospace, and telecom applications

Where appropriate, supported actions shall promote open standards, open interfaces, open-source design tools and open processor architectures, including RISC-V, in order to reduce vendor lock-in, improve auditability, strengthen cybersecurity and facilitate participation by SMEs, start-ups, public administrations and research and knowledge-dissemination organisations.

Implementation may take the form of a large-scale public-private partnership mobilising EUR 8-12 billion in combined EU, Member State, and private funding, structured around consortia centred around fabless semiconductor firms, and involving ASIC design houses, Electronic Design Automation tool vendors, IP providers, research ~~institutes~~**and knowledge-dissemination organisations**, and end-user industries (automotive and aeronautical Original Equipment Manufacturers, telecom operators, defence primes). Investment shall cover chip architecture and design teams, advanced design tools and IP libraries, prototyping, verification, software stacks, and industrialisation. The project shall have guaranteed access to advanced fabrication through partnerships with leading foundries or European pilot lines at 2nm and below. A phased approach may begin with capability mapping and target application selection, followed by design and validation programmes, pilot tape-outs, ecosystem development, and commercial deployment, alongside dedicated measures to develop talent and attract world-class engineering expertise. **Participation of research and knowledge-dissemination organisations, competence centres and innovative SMEs should be encouraged throughout the project lifecycle.**

PUBLIC

A call for expression of interest may invite proposals from industrial consortia for leading-edge chip design projects with clear strategic relevance, asking applicants to specify the target application domain, expected technological differentiation, required investment, access to design and manufacturing infrastructure, timeline to prototype and commercialisation, and contribution to Europe's resilience**, technological sovereignty** and competitiveness.

6. Strengthening key segments of the value chain

The Union faces several vulnerabilities in the semiconductor value chain. Many of these vulnerabilities are well-known, including the ones above, whereas others are less obvious and/or considered less critical. The latter vulnerabilities may come to the surface when certain events take place, revealing their full impact and exposing dependencies, as witnessed in the Nexperia case (see Staff Working Document).

It will not be feasible or practical for the Union to address all possible vulnerabilities in the semiconductor value chain. However, it may be desirable for the Union to have the possibility to reduce some vulnerabilities and strengthen key segments of the value chain, especially when disruptions demonstrated dependencies or when such disruptions are likely to happen.

PUBLIC

This type of strategic projects aims to strengthen a particular key segment of the semiconductor value chain. Such interventions shall not be limited to the most advanced parts of the value chain, and may address, for instance, the production of mainstream chips, back-end processes, Printed Circuit Board (PCB) **production and** assembly, **advanced packaging, integrated-circuit substrates, electronics manufacturing services and system integration** and also materials and equipment. An example of a potential strategic project may be the setup of an OSAT[2] facility that would predominantly cater for European user industries. Another example may be the setup of an advanced packaging facility that would complement (new) front-end fabs. The main participants in strategic projects shall be companies headquartered in the Union, and prime investment shall typically, but not necessarily always, take place in the Union. **Support for these segments shall be based on an identified strategic dependency, market failure or sub-optimal investment situation and shall demonstrate clear Union added value.**

This type of strategic projects shall address suspected and proven vulnerabilities in the semiconductor value chain. Using targeted actions to strengthen key segments of the value chain shall increase Europe's technological sovereignty and reduce dependencies on foreign actors.

The European Semiconductor Board shall have a key role in selecting the areas of the value chain where strengthening is needed. As a next step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

PUBLIC

[2] OSATs – Outsourced Semiconductor Assembly and Test – are third-party service providers who specialise in the final, critical stages of chip manufacturing, i.e. packaging the semiconductor die and testing it for functionality before it reaches customers.

1f. Photonic chips and integrated photonics

Photonics is a key enabling technology for the semiconductor value chain and a natural extension of the Chips for Europe Initiative. As electrical interconnects reach their bandwidth and energy limits, optical transmission is moving into the package itself, making co-packaged optics and optical input/output a precondition for scaling artificial intelligence compute and data centres. Photonic integrated circuits (PICs) are equally indispensable for fibre-optic and 5G/6G networks, satellite and free-space laser communication, LiDAR and industrial sensing, medical diagnostics, and for quantum computing, communication and sensing. The Union has a world-leading research base, mature technology platforms in indium phosphide, silicon nitride and silicon-on-insulator, and strong positions in lasers, optical equipment and materials, reinforced by the pilot line for advanced photonic integrated circuits established under the Chips Act. These strengths are not matched by industrial capacity. The Union has no high-volume PIC manufacturing at scale and only very limited capacity for photonic packaging, assembly and testing, which is the most cost-determining stage of a photonic product. It depends on non-EU suppliers for laser light sources, for the high-speed driver, receiver and digital signal processing chips that accompany photonic circuits, and for most optical transceiver modules deployed in European networks. European photonics companies consequently scale and relocate outside the Union, and the value created by European research is captured elsewhere.

PUBLIC

This strategic project aims to convert the Union's research and pilot-line strengths in integrated photonics into industrial capacity. It shall establish first-of-a-kind high-volume PIC manufacturing, heterogeneous integration and photonic packaging, assembly and test capacity in the Union, covering co-packaged optics and photonic chiplets for artificial intelligence compute, European light sources and their integration on silicon, optical transceivers for networks and space communication, photonic chips for sensing, imaging and diagnostics, quantum photonics, and the design ecosystem of process design kits, design automation tools and prototyping services for fabless photonic companies. Public and private investments are estimated between EUR 4 and 8 billion depending on the option chosen, building on the pilot lines of the Chips for Europe Initiative and retaining the resulting intellectual property in the Union.

This strategic project shall reduce structural dependencies on non-EU suppliers of photonic components, light sources and optical modules, increase supply security for artificial intelligence infrastructure, connectivity, mobility, healthcare, space and defence, and retain in the Union both the economic value and the companies emerging from European photonics research. It shall also improve the energy efficiency of European digital infrastructure and strengthen the Union's position in quantum technologies, for which integrated photonics is a critical enabler.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

PUBLIC

ANNEX III

Measurable indicators to monitor the implementation and to report on the progress of this Regulation towards the achievement of its objectives

The Commission shall be responsible for monitoring the implementation of this Regulation on a regular basis, possibly with the support of external studies, Member State and market data. The Commission shall carry out a comprehensive evaluation of the effectiveness, efficiency, coherence, proportionality, and subsidiarity of this Regulation. An evaluation report presenting the main findings shall be submitted to the European Parliament, the Council, the European Economic and Social Committee, and the Committee of the Regions in line with Article 60 of this Regulation. Where appropriate, the Commission may accompany this report with proposals for improving or adapting this Regulation.

The Commission, in close cooperation with the Member States, shall regularly monitor the implementation and application of the legal provisions, with particular attention to the effectiveness of the adopted measures. Monitoring activities shall rely on quantitative and qualitative indicators, drawing from data provided by stakeholders across the semiconductor value chain, Member States, and relevant Union bodies. **Monitoring activities shall be designed so as to minimise administrative burden on Member States and stakeholders. The Commission shall, to the extent possible, rely on existing Union and national data sources, market data and already established reporting mechanisms. Additional data requests to Member States shall be limited to what is strictly necessary, proportionate and clearly linked to the objectives of this Regulation.**

The measurable indicators shall build on the two general objectives of this Regulation.

General monitoring indicators:

- total semiconductor related FDI inflows into the Union;
- skilled workforce in ~~semiconductor and photonics~~**chips**, including workforce trained/reskilled through the national chips competence centres' initiatives;

- public support to start-ups and scale ups**, SMEs and small mid-caps operating across the semiconductor value chain**; and

- scale-up funding via private equity and Venture Capital.

Specific monitoring indicators:

First specific monitoring indicators for enhancing the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips:

- Union share of global semiconductor value (in EUR) in the different segments of the value chain:

- design, IP, EDA; **photonic integrated circuit design and other strategic semiconductor design activities;**

- manufacturing;

- equipment manufacturing;

- OSAT (Packaging);

- materials / gases;

- top Union firms in any value chain segment;

- installed wafer fabrication capacity in the Union (wpm).

Second specific monitoring indicator for developing a strong user market across key industry sectors: Consumption of chips by key sectors (automotive, energy, health, defence, telecom, AI/data centres/cloud) in value (EUR)**, including uptake of semiconductor technologies developed within the Union**.

PUBLIC

Third specific monitoring indicator for increasing intelligence capabilities for crisis preparedness and response: Coverage (in %) of the Union semiconductor value chain monitored by the Business-to-Business Semiconductor Supply Chain Platform.

PUBLIC

ANNEX IV

Synergies of this Regulation with other programmes

(1) Synergies of the Chips for Europe Initiative 2.0 with the Specific Objectives 1 to 5 of the Digital Europe Programme shall ensure that:

(a) the targeted thematic focus of the Chips for Europe Initiative 2.0 on ~~semiconductor and quantum~~**chip** technologies is complementary;

(b) Specific Objectives 1 to 5 of the Digital Europe Programme support digital capacity building in the advanced digital technologies, including High Performance Computing, AI and cybersecurity, and advanced digital skills;

(c) The Chips for Europe Initiative 2.0 will invest in capacity building to reinforce advanced design, production and systems integration capabilities in cutting-edge ~~semiconductor~~**chip** technologies, next-generation ~~semiconductor~~**chip** technologies and cutting-edge quantum technologies for innovative business development, strengthening the Union's semiconductor supply and value chains, serving key industrial sectors and creating new markets.

(2) Synergies with Horizon Europe shall ensure that:

(a) although thematic areas addressed by the Chips for Europe Initiative 2.0 and several areas of Horizon Europe converge, the type of actions to be supported, their expected outputs and their intervention logic are different and complementary;

(b) Horizon Europe provides extensive support for research, technological development, demonstration, piloting, proof-of-concept, testing and prototyping, including pre-commercial deployment of innovative digital technologies, in particular through:

(i) a dedicated budget in the pillar 'Global Challenges and European Industrial Competitiveness' for the cluster 'Digital, Industry and Space' to develop enabling technologies (AI and robotics, Next Generation internet, High Performance Computing and Big Data, key digital technologies (incl. microelectronics), combining digital with other technologies);

(ii) support to research infrastructures under the pillar 'Excellent Science';

(iii) the integration of digital across all the Global Challenges (health, security, energy and mobility, climate, etc.); and

(iv) support for scale-up breakthrough innovations under the pillar 'Innovative Europe' (many of which will combine digital and other technologies).

(c) the Chips for Europe Initiative 2.0 is exclusively focusing on building large-scale capacities in ~~semiconductor and quantum~~**chip** technologies across the Union. It will invest in:

(i) fostering innovation by supporting two closely interlinked technological capacities that enable designing novel system concepts and their testing and validation in pilot lines**, while facilitating technology transfer**;

(ii) providing targeted support to build training capacity and enhance applied advanced digital competences and skills to support development and deployment of ~~semiconductors~~**chips** by technology development and end-user industries; and

(iii) a network of national competence centres, which facilitate access and provide expertise and innovation services to end-user communities and industries, to develop new products and applications and to address market failures.

(d) the technology capacities of the Chips for Europe Initiative 2.0 will be made available to the research and innovation community, including for actions supported through Horizon Europe;

(e) as the development of novel digital technologies in the area of ~~semiconductors~~**chip technologies** matures through Horizon Europe, those technologies where possible progressively will be taken up and deployed by the Chips for Europe Initiative 2.0;

PUBLIC

(f) the Horizon Europe programmes established under Regulation (EU) 2021/695 for the development of skills and competencies curricula, including those delivered at the co-location centres of the European Institute of Innovation & Technology's Knowledge and Innovation Communities, are complemented by capacity building in advanced applied digital skills and competences in ~~semiconductor and quantum~~**chip** technologies supported by the Chips for Europe Initiative 2.0;

(g) strong coordination mechanisms for programming and implementation are put in place, aligning all procedures for both Horizon Europe and the Chips for Europe Initiative 2.0 to the extent possible; their governance structures will involve all Commission services concerned **and should, where appropriate, facilitate synergies with national semiconductor strategies and programmes of the Member States**.

(3) Synergies with the proposed Cloud and AI Development Act (CADA) **and European High Performance Computing (EuroHPC) Joint Undertaking** shall contribute to a coherent approach to strengthening the Union's technological sovereignty, by addressing both the supply of and demand for advanced ~~semiconductor~~**chip** technologies, in particular through:

(a) leveraging demand for ~~semiconductors~~**chips** stemming from cloud and AI development: this Regulation shall support the capacity of the Union to respond to the demand of high-performance and energy-efficient ~~semiconductors~~**chips** generated by the expansion of cloud and AI infrastructure, including data centres and large-scale computing facilities;

(b) supporting the deployment of AI Factories and AI Gigafactories: this Regulation shall support the availability of advanced and specialised ~~semiconductors~~**chips** required for high-performance computing and artificial intelligence applications, thereby enabling the deployment and scaling of AI Factories and AI Gigafactories in the Union and contributing to industrial-scale AI development and scientific capabilities.

(c) supporting secure and resilient digital infrastructures: this Regulation shall contribute to ensuring the availability of components needed for the development of trusted and sovereign cloud and AI environments for critical use cases needed to increase reliance on secure and reliable hardware components by strengthening the resilience and security of semiconductor value chains.

(d) supporting the deployment of digital infrastructures based on Union technological capabilities and ~~reduce~~**reducing** exposure to external dependencies **across strategic segments of the semiconductor value chain**;

(e) contributing to sustainability objectives of digital infrastructure deployment: this Regulation shall support the development and production of resource-efficient and energy-efficient ~~semiconductors~~**chips** in order to address the growing deployment of data centres and cloud infrastructure which is expected to increase demand for energy-efficient digital technologies; **such support shall be accompanied by lifecycle-based assessment of energy, water, cooling, land-use and grid impacts of cloud, AI and datacentre deployment, and shall prioritise solutions that demonstrably reduce total system-level resource consumption;**

(4) Synergies with Union programmes under shared management, including the European Regional Development Fund, the European Social Fund Plus, the European Agricultural Fund for Rural Development and the European Maritime, Fisheries and Aquaculture Fund, shall ensure the development and strengthening of regional and local innovation ecosystems, industrial transformation, as well as the digital transformation of society and of public administrations. This includes support for the digital transformation of industry and the take-up of results, as well as the rolling out of novel technologies and innovative solutions. The Chips for Europe Initiative 2.0 will complement and support the transnational networking and mapping of capacities it will support and make them accessible to SMEs and end-user industries in all Union regions.

(5) Synergies with the Connecting Europe Facility shall ensure that:

(a) the Chips for Europe Initiative 2.0 focuses on large-scale digital capacity and infrastructure building in the areas of semiconductors aiming at the wide uptake and deployment across the Union of critical existing or tested innovative digital solutions within a Union framework in areas of public interest or market failure. The Chips for Europe Initiative 2.0 is mainly to be implemented through coordinated and strategic investments with Member States, in building digital capacities in ~~semiconductor~~**chip** technologies to be shared across the Union and in Union-wide actions. This is particularly relevant in electrification and autonomous driving, and is intended to benefit and facilitate the development of more competitive end-use industries, particularly in the mobility and transport sectors; **such capacities should be accessible to a broad range of stakeholders from across the Union;**

(b) the capacities and infrastructures of the Chips for Europe Initiative 2.0 are to be made available to testing of innovative new technologies and solutions that can be taken up in the mobility and transport industries. The Connecting Europe Facility is to support the roll-out and deployment of innovative new technologies and solutions in the field of mobility and transport as well as in other domains;

(c) coordination mechanisms are to be established, in particular through appropriate governance structures.

(6) Synergies with InvestEU Programme shall ensure that:

(a) support through market-based financing, including pursuing policy objectives under the Chips for Europe Initiative 2.0 is provided by Regulation (EU) 2021/523; such market-based financing might be combined with the grant support;

(b) a blending facility under the InvestEU Fund is supported by financing provided by Horizon Europe or the Digital Europe Programme in the form of financial instruments within blending operations.

PUBLIC

(7) Synergies with Erasmus+ shall ensure that:

(a) the Chips for Europe Initiative 2.0 supports the development and acquisition of the advanced digital skills needed for the development and deployment of cutting-edge ~~semiconductor~~**chip** technologies in cooperation with relevant industries; **research and knowledge-dissemination organisations and competence centres;**

(b) the advanced skills part of Erasmus+ complements the interventions of the Chips for Europe Initiative 2.0, addressing the acquisition of skills in all domains and at all levels through mobility experiences.

(8) Synergies with other Union programmes and initiatives on competencies and skills shall be ensured.

(9) Synergies with Union cybersecurity legislation shall ensure that:

(a) investments supported under the Chips for Europe Initiative 2.0 contribute to strengthening the security and resilience of semiconductor supply chains in the Union;

(b) the Chips for Europe Initiative 2.0 complements the objectives of the Cyber Resilience Act and the EU Cybersecurity Act by supporting the development and deployment of trusted ~~semiconductor~~**chip** technologies;

(c) coordination is ensured with the implementation of Directive (EU) 2022/2555 (Network and Information Security Directive, NIS2), including where appropriate the promotion of trusted chips in critical sectors.

(10) Synergies with Important Projects of Common European Interest (IPCEIs) and relevant State aid frameworks shall ensure that:

(a) actions supported under the Chips for Europe Initiative 2.0 remain coherent with existing State aid and competition rules, including the R&D&I Framework and the IPCEI Communication;

PUBLIC

(b) IPCEIs, including the IPCEI candidate on Advanced Semiconductor Technologies (AST), may contribute to bridging research and innovation activities with industrial deployment and manufacturing capacities~~, thereby complementing the objectives of the Chips for Europe Initiative 2.0~~;

(c) the Chips for Europe Initiative 2.0 addresses complementary investment gaps to the support of first-of-a-kind semiconductor manufacturing facilities and related technological capacities.

(11) Synergies with national semiconductor strategies, roadmaps and investment plans shall ensure that:

(a) Member States' national semiconductor strategies and investment plans are aligned with the objectives of the Chips for Europe Initiative 2.0**, while respecting national priorities and strengths**;

(b) national and Union investments contribute to strengthening regional and cross-border semiconductor ecosystems across the Union;

(c) coordination mechanisms support the mapping of semiconductor capacities and facilitate cooperation between Member States in order to strengthen the resilience of the Union's semiconductor value chains and avoid unnecessary duplication of investments **and maximise complementarities between national and Union initiatives**.

PUBLIC

ANNEX V

Critical Sectors

(1) Energy

(2) Transport

(3) Banking

(4) Financial market infrastructure

(5) Health

(6) Drinking water

(7) Waste water

(8) Digital infrastructure

(9) Public administration

(10) Space

(11) Production, processing and distribution of food

(12) Defence

(13) Security

PUBLIC

ANNEX VI Industrial sectors using semiconductors

PUBLIC

(1) Automotive

(2) Datacentres, cloud and AI

(3) Industrial automation and robotics

(4) Aeronautics

(5) Space, defence and security

(6) Electronic communications infrastructures

(7) Industrial-grade computing and IoT

(8) Health care and medical devices

(9) Electronic manufacturing services providers and distributors

(10) Renewable and low carbon energy systems