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PART 1/3

COMMISSION STAFF WORKING DOCUMENT

IMPACT ASSESSMENT REPORT

Accompanying the document

Proposal for a Regulation of the European Parliament and of the Council

on a framework of measures for strengthening Europe's semiconductor ecosystem repealing Regulation (EU) 2023/1782 (Chips Act 2.0)

{COM(2026) 504 final} - {SEC(2026) 504 final} - {SWD(2026) 505 final}

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Glossary

Term or acronym	Meaning or definition
Advanced nodes	Semiconductor manufacturing processes at the leading edge of miniaturisation, conventionally referring to nodes at or below 7nm. They deliver higher performance and energy efficiency and are primarily used for high-performance computing, AI accelerators and flagship mobile processors. Note that modern node designations no longer correspond to a specific physical transistor dimension.
AI chips	Logic chips optimised for the matrix and tensor operations that underpin machine-learning training and inference. The category includes GPUs, dedicated AI accelerators (e.g. TPUs, NPUs), FPGAs and purpose-built ASICs.
Back-end	The stages of semiconductor manufacturing that follow wafer fabrication, comprising dicing, assembly, packaging and test of the finished device.
Chiplet	A small, independent die designed to perform one or more specific functions and intended to be combined with other chiplets within a single advanced package, allowing modular design and mixing of process nodes.
Chips for Europe Initiative	The framework established under Pillar I of the Chips Act to build large-scale technological capacity and support research and innovation across the Union's semiconductor value chain. It covers design capacities, pilot lines, quantum chips, competence centres and access to finance.
Competence centre	Facilities forming a Union-wide network, at least one per Member State, that provide access to design services, pilot lines, expertise and training to support stakeholders in the semiconductor ecosystem, in particular SMEs. They facilitate technology transfer, skills development, and links between students and semiconductor companies across the Union.
Compound semiconductors	Semiconductors made from two or more chemical elements, in contrast to elemental semiconductors such as silicon. Key examples include silicon carbide (SiC) and gallium nitride (GaN), used in power electronics and RF applications, and gallium arsenide (GaAs) and indium phosphide (InP), used in optoelectronics and high-frequency communications. They offer performance characteristics such as high voltage, high frequency, high temperature tolerance, that silicon cannot match, and are strategically important for automotive electrification, renewable energy and telecommunications.

Deep Ultraviolet lithography (DUV)	A lithography technology using ultraviolet light at 248nm or 193nm wavelengths (the latter typically in an immersion configuration) to pattern wafers. DUV remains the workhorse of semiconductor manufacturing for mature nodes and, with multi-patterning techniques, can produce features down to around the 7nm node.
Design Centre of Excellence	A label that may be awarded by the Commission to design centres established in the Union that significantly enhance the Union's capabilities in innovative chip design, either through their service offerings or through the development, promotion and strengthening of design skills. Such centres are recognised as serving the public interest and contributing to the resilience of the Union's semiconductor ecosystem.
Electronic Design Automation (EDA)	The category of software tools used to design, simulate, verify and prepare for manufacturing the integrated circuits and printed circuit boards that make up electronic systems. EDA tools are indispensable to modern chip design, particularly at advanced nodes, and the market is highly concentrated among a small number of global suppliers.
European Semiconductor Board (ESB)	The governance body composed of high-level representatives of all Member States and chaired by the Commission, responsible for facilitating implementation of, cooperation under and information exchange relating to the Chips Act, including advising on international cooperation, crisis response, and the assessment of integrated production facilities and open EU foundries.
Extreme Ultraviolet lithography (EUV)	A lithography technology using 13.5nm wavelength light to pattern the finest features on advanced-node wafers. EUV is essential for manufacturing at and below the 7nm node and is supplied globally by a single company (ASML, headquartered in the Netherlands), making it a strategic chokepoint in the semiconductor value chain.
Fabless	A semiconductor company that designs and sells integrated circuits but does not own or operate a wafer fabrication plant, instead outsourcing manufacturing to a foundry. The fabless model separates design from production and is the counterpart to the foundry model.
First-of-a-kind facility (FOAK)	A new or substantially upgraded semiconductor manufacturing facility, or a facility for the production of equipment or key components for such equipment predominantly used in semiconductor manufacturing, which provides innovation with regard to the manufacturing process or final product that is not yet substantively present or committed to be built within the Union. The innovation may concern improvements in computing power, security, safety or reliability, energy and environmental performance, the

	technology node or substrate materials, production-process efficiency, recyclability, or the reduction of production inputs.
Foundry	A semiconductor manufacturing company that fabricates wafers on behalf of other firms, typically fabless companies, IDMs or system companies, according to their designs, without selling chips under its own brand. A pure-play foundry undertakes no design of its own.
Front-end	The stages of semiconductor manufacturing from a blank wafer through to a completed, patterned wafer, comprising lithography, etching, deposition, doping and related process steps.
Heterogeneous integration	The assembly and interconnection within a single advanced package of multiple components, such as chiplets, memory stacks, photonic devices or sensors, that may be produced on different process technologies or from different materials. It is a leading alternative to traditional monolithic scaling and underpins the chiplet ecosystem.
Important Projects of Common European Interest (IPCEI)	Large-scale projects bringing together companies and research centres from several Member States to deliver significant benefits to strategic EU goals such as competitiveness, sustainable growth, addressing societal challenges and creating value across the Union.
Integrated Device Manufacturers (IDMs)	Semiconductor companies that design, manufacture (in their own fabs) and sell integrated-circuit products, in contrast to the fabless–foundry model.
IP block	A reusable, pre-designed and pre-verified unit of logic, cell or chip layout that can be licensed and integrated into a larger integrated-circuit design. Also referred to as a semiconductor IP core or design IP, IP blocks (e.g. CPU cores, memory controllers, interface PHYs) shorten design cycles and are a key input to modern system-on-chip development.
Lithography	The patterning step in semiconductor manufacturing in which the circuit design is transferred onto the wafer using light projected through a mask onto a light-sensitive coating (photoresist). Lithography is the principal driver of feature-size scaling and one of the most capital-intensive and technologically demanding steps in chip production.
Mature technology nodes	Established semiconductor manufacturing processes, conventionally referring to nodes at or above 28nm. They offer lower cost, high production stability and long product lifecycles, and remain dominant in high-volume applications such as automotive electronics, power management, industrial controls and consumer products. Also referred to as legacy nodes.

Memory chips	Semiconductor devices designed to store data, distinct from logic chips, which process it. The main families are DRAM (dynamic random-access memory, used as main system memory), NAND flash (non-volatile storage for SSDs and mobile devices) and NOR flash (typically used for code storage).
Microcontroller (MCU)	A small, self-contained integrated circuit combining a processor core, memory and input/output peripherals on a single chip, designed for embedded control applications. MCUs are produced predominantly at mature nodes and are central to automotive, industrial and consumer electronics. Shortages of automotive MCUs were a defining feature of the 2021–2023 semiconductor crisis.
Moore's Law	The empirical observation, formulated by Gordon Moore in 1965 and revised in 1975, that the number of transistors on an integrated circuit doubles roughly every two years. Although it is not a physical law, it has served for decades as a guiding target for the industry and as a proxy for progress in cost, performance and energy efficiency. The pace of scaling has slowed at advanced nodes, prompting greater emphasis on architectural innovation, advanced packaging and heterogeneous integration.
Original Equipment Manufacturers (OEMs)	Companies that produce systems or components which are integrated into another company's end product. In the semiconductor context, OEMs typically incorporate chips and modules supplied by others into the products they design, brand and sell.
Photonic chips	Integrated circuits that process or transmit information using light (photons) rather than, or in addition to, electrical signals. Silicon photonics i.e. photonic devices fabricated using CMOS-compatible silicon processes, is a particularly active area, with applications in high-bandwidth data-centre interconnects, telecommunications, sensing and emerging quantum technologies.
Pilot line	An experimental project or experimental production addressing higher technology readiness levels (TRL 3 to 8), used to further develop the enabling infrastructure required to test, demonstrate, validate and calibrate a product or system against its model assumptions.
Quantum chips	Integrated devices that exploit quantum-mechanical phenomena such as superposition and entanglement to perform computation, sensing or communication tasks. Several physical implementations are under active development, including superconducting circuits, trapped ions, photonic platforms and silicon-spin qubits. Quantum chips are explicitly supported under Pillar I of the Chips Act.

Substrate	The underlying material on which semiconductor devices are fabricated. The dominant substrate is monocrystalline silicon, supplied as wafers; other substrates include silicon carbide and gallium nitride (for power and RF devices), gallium arsenide and indium phosphide (for optoelectronics), and silicon-on-insulator (SOI) variants for specialised applications. The choice of substrate determines key device characteristics and constrains the available process technology.
System-on-Chip (SoC)	An integrated circuit that combines on a single die all the major functional components of a complete electronic system — typically including one or more processor cores, memory, input/output interfaces and specialised accelerators. SoCs are common in smartphones, embedded systems and increasingly in automotive and AI applications, and are usually assembled from a mix of in-house and licensed IP blocks.
Technology node	A designation referring to a specific semiconductor manufacturing process generation and its associated design rules. Historically tied to a physical transistor dimension (notably gate length), the term is today primarily a marketing and benchmarking label that signals a generation of performance and density rather than a measurable feature size.
Transistor	The fundamental building block of modern integrated circuits: a semiconductor device that acts as an electronic switch or amplifier by controlling current flow between two terminals through a voltage or current applied to a third. Billions of transistors, typically of the MOSFET family (including FinFET and gate-all-around variants at advanced nodes), are integrated on a single chip.
Yield	The proportion of functional dies produced on a wafer relative to the maximum theoretical number. Yield is a critical determinant of the unit cost and economic viability of a semiconductor process, particularly at advanced nodes where defect sensitivity is high and a single fab can represent investments of well over EUR 10 billion.

1 INTRODUCTION: POLITICAL AND LEGAL CONTEXT

1.1 Political context

Semiconductors underpin all digital technologies from household appliances to defence equipment to the data centres at the core of the artificial intelligence (AI) revolution. Since 2020, a series of shortages of supply stemming from crises, such as the COVID-19 pandemic, disruptions, such as the recent Nexperia case, and the ongoing supply-demand mismatch in the memory market expose how excessive external dependencies can render entire markets vulnerable. Increased geopolitical rivalry, including Sino-American tensions, and the emergence of AI have further amplified the crucial role of semiconductors, which have become a strategic asset in geopolitics. Without question, chips occupy an essential place in the global technological race.

Semiconductors are the third most traded commodity globally (after oil and vehicles), reaching revenues of USD 700.9 billion in 2025([1]). It is widely expected that the market size of the semiconductor industry will reach USD 1 trillion by 2026([2]). The industry's role as a critical supplier to most modern industries and to the infrastructure that supports the rest, has elevated it to an important strategic resource which, in a more transactional world, can be a source of geopolitical leverage. Regions without significant capabilities in this domain find themselves dependent on components that others can restrict or condition in an increasingly coercive global environment.

The European Chips Act, which has been in force since September 2023, has served as a catalyst for renewed momentum and investment in the European semiconductor industry. It is a prime example of a new wave of European industrial policies and was conceived to reinforce the semiconductor ecosystem in the EU, ensure the security of supply chains and reduce external dependencies. It focuses on **five strategic objectives**:

1. Strengthening research and technological leadership
2. Building and reinforcing the EU's capacity to innovate in the design, manufacturing and packaging of advanced chips
3. Putting in place an adequate framework to increase production by 2030
4. Addressing the skills shortage and attracting new talent
5. Developing an in-depth understanding of global semiconductor supply chains

Under Pillar I of the Chips Act, the *Chips for Europe Initiative*([3]), over 85% of the Union's budget has been committed to the deployment of five pilot lines, a network of competence centres in all Member States, a Design Platform, six quantum chip pilot lines, skills development activities and scale-up investment in start-ups via the Chips Fund([4]).

([1]) WSTS Semiconductor Market Forecast Spring 2025
([2]) Global chip sales expected to hit $1 trillion this year, industry group says | Reuters
([3]) European Chips Act: The Chips for Europe Initiative | Shaping Europe's digital future
([4]) A detailed analysis of these initiatives and the state of play of the implementation can be found in the annexed Evaluation of the Chips Act.

Through Pillar II([5]), the Chips Act has triggered around EUR 80 billion in announced or planned manufacturing investments in the Union. Key projects include the **European Semiconductor Manufacturing Company's (ESMC)** fab in Dresden (Germany) - bringing FinFET technology ([6]) to the EU; the **SiliconBox** facility in Novara (Italy) - a first advanced packaging facility in the EU; and the **STMicroelectronics Silicon Carbide (SiC) campus in Catania** (Italy) - now the world's largest SiC facility.

By the end of 2025, the Commission had approved eleven First-of-a-Kind projects, worth over EUR 31.6 billion of public and private investment. These projects include investments in mainstream semiconductor technologies to meet the needs of key European user industries, such as automotive([7]). Once these investments materialise, it is expected that the manufacturing capacity of the Union will increase by 30%, from 1.07 million wafers per month in 2023 to over 1.39 million wafers per month in 2030.([8])

As part of the activities under Pillar III of the Chips Act([9]), through the European Semiconductor Board (ESB), the Commission and Member States are coordinating more closely their activities and jointly building a crisis response mechanism, as set out in the Regulation.

Nevertheless, despite this considerable progress and the Union's strengths in key segments of the semiconductor value chain such as mainstream semiconductor production (including power electronics, embedded systems components, photonics, sensors), manufacturing equipment and materials, clear gaps in capabilities still need to be addressed. To this end, the EU must double down on its efforts to create an investment environment that is conducive for advanced front-end manufacturing, advanced packaging and heterogeneous integration fabs, as well as the ramp-up of leading-edge design activities, while maintaining a strong and competitive industry for more mature technologies. The vulnerabilities generated by these capability gaps become more consequential as productivity gains from the deployment of AI become more pronounced([10]).

Since the adoption of the Chips Act, the dynamics of the semiconductor market have shifted drastically, with AI becoming the key driver of revenues. Over the past two years, market growth has been largely driven by chips for AI datacentres (processors, memory), whilst most other segments have remained stagnant. This trend is expected to continue. According to McKinsey ([11]), between 2023 and 2030, the AI logic chip segment is projected to grow at a compound annual growth rate (CAGR) of 18-29%, while AI memory chips are expected to grow at a CAGR of 17-23%, in contrast to most other semiconductor segments (excluding the China market) that are likely to show a more subdued performance, with average growth of

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([5]) European Chips Act: Security of supply and resilience | Shaping Europe's digital future
([6]) The FinFET (Fin Field Effect Transistor) process is a 3D process adopted to overcome the limitations of conventional planar (2D) transistor structures and is used mostly for technology nodes between 16nm and 5nm.
([7]) JRC, EU's strengths and weaknesses in the global semiconductor sector, 2025
([8]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report. Risks here include economic downturns or market turbulations.
([9]) European Chips Act: Monitoring and crisis response | Shaping Europe's digital future
([10]) The AI productivity take-off is finally visible
([11]) AI's uneven impact on semiconductor industry market share | McKinsey

around 3%. For the foreseeable future, AI-related components are expected to drive growth, and as seen in Figure 1, they should represent over 70% of the total semiconductor market by 2030([12]).

This shift in market dynamics is coupled with the stark reality that the EU finds itself without the sovereign means to compete effectively in a world where access to advanced AI technologies is becoming a key determinant of competitiveness. Unlike its main global competitors, the EU lacks the capacity necessary to capture a meaningful share of the rapidly expanding AI-driven market. As a result, the Union's dependence on third country suppliers for cutting-edge semiconductor manufacturing is near-total, exposing critical downstream industries to significant supply chain vulnerabilities and risks.

This needs to be addressed alongside continued consolidation of current European strengths that are crucial for important industrial verticals in the EU, such as automotive, industrial automation, aerospace and defence, and telecommunications. These however require relatively small volumes of semiconductors that are unable to sustainably maintain a viable semiconductor manufacturing ecosystem on their own, especially at more leading-edge technologies. Therefore, to safeguard the security of supply of these critical sectors, more needs to be done to stimulate demand in other sectors, which then create the conditions for a sustainable ramp-up of supply.

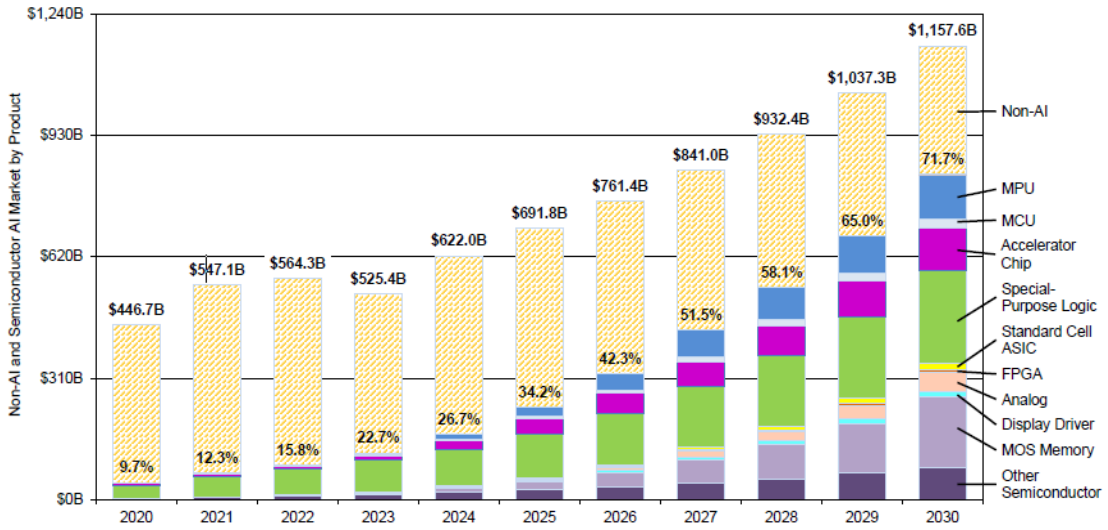

Figure 1 - Total Semiconductor Market and AI-related Share by Product (Source: IBS)[13]

To this end, humanoid robots and wearables are emerging application areas that are expected to generate significant future demand for semiconductors ([14]). Although both markets remain relatively small today, their projected growth is a sign of potential over the medium to long term until 2035-2040 and the EU could benefit from it. While industrial robots are already crucial factors in deploying automation in factories, humanoid robots are expected to expand

([12]) IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.
([13]) IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.
([14]) McKinsey | The next big arenas of competition

rapidly due to their potential in services, care, and human–machine interaction. The global semiconductor market for humanoid robots is estimated at EUR 360 million in 2024, and, under an optimistic uptake scenario, it is projected to grow at 26.2% annually to reach EUR 4.7 billion by 2035 ([15]). In the EU27, direct semiconductor consumption is estimated at EUR 70 million in 2024, increasing to EUR 770 million by 2035 (23.8% annual growth). Wearables constitute a second future-oriented market, combining consumer and healthcare applications. The global semiconductor market for wearables amounts to EUR 17 billion in 2024 and is expected to grow at 6.3% annually, reaching EUR 33.2 billion by 2035 ([16]).

Both applications present an opportunity for Europe since they require compute capacity at the edge, an area where the Union has considerable expertise and know-how. This will however require significant private investment, stimulated by public support, to ensure that incumbent and upcoming semiconductor suppliers in the EU are in a position to capture significant shares of these future markets. A robust semiconductor industry in the Union requires a three-pronged approach that carves out a space for European semiconductor solutions in the AI ecosystem, consolidates current strengths, and ventures into new markets

Against this backdrop, both Member States and the European Parliament have called for a renewed impetus to the EU's efforts in the field of semiconductors. Through the '*Semicon Coalition'* ([17]), all 27 EU Member States have called for a coordinated approach to ensure prosperity, indispensability and resilience:

- **Prosperity:** enabling a competitive European semiconductor ecosystem that enhances Europe's economic welfare and value creation across end-markets.
- **Indispensability**: maintain and develop Europe's technological and innovation leadership to secure critical control points in the global semiconductor value chain.
- **Resilience:** secure a stable and reliable supply of trustworthy semiconductors for Europe's most critical sectors, particularly in times of global disruption or geopolitical uncertainty.

In March 2025, 54 Members of the European Parliament signed a letter ([18]) to the Commission calling for a revised Chips Act, with a core focus on "*AI chips and other semiconductor technologies that were not adequately covered under the initial proposal*". Similarly, the European Parliament adopted an own-initiative report on European Technological Sovereignty and Digital Infrastructure ([19]) calling for urgent action to boost EU domestic semiconductor manufacturing, to put advanced AI chips at the core of the revision of the Chips Act, and to adapt the Chips Act to the architecture of the proposed Multiannual

([15]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.
([16]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.
([17]) Semicon Coalition calls for reinforced Chips Act | Shaping Europe's digital future
([18]) MEPs urge the Commission to propose a Chips Act 2.0 | Euractiv
([19]) REPORT on European technological sovereignty and digital infrastructure | A10-0107/2025 | European Parliament

Financial Framework (MFF), particularly to the European Competitiveness Fund proposal ([20]).

1.2 Relevant existing EU legislation and related initiatives

Semiconductors are critical enablers of the green and digital transitions, and their strategic importance for the EU is further amplified by geopolitical tensions, the Union's current over-dependence on advanced manufacturing and design, and the increasing weaponisation of these dependencies by third countries. In this context, Chips Act 2.0 is indispensable to the achievement of the Commission's political priorities, notably "*A new plan for Europe's sustainable prosperity and competitiveness*" and "*A new era for European defence and security*".

In the aftermath of the **Draghi report** ([21]), competitiveness became a central component of the Commission's political priorities for 2024-2029 ([22]), triggering a series of initiatives. The report singled out semiconductors as a key sector in which Europe needs to close the innovation gap, contribute to a joint decarbonisation and competitiveness plan, increase security, and reduce dependencies. In his report, Prof. Draghi called for a new, better articulated and concerted approach to boost the EU's future competitiveness in this sector by "*developing a comprehensive EU Semiconductor Strategy, supported by a dedicated EU-level budget for semiconductors; enhanced funding for innovation, including grants or R&D tax incentives for fabless chip design companies and for foundries operating in strategically relevant segments"*. Prof. Draghi's report also called for coordinated EU action in **back-end 3D advanced packaging**, **advanced materials**, and **finishing processes**[23], as well as the establishment of an **EU-wide**, streamlined, and investment-friendly **permitting regime** for semiconductor manufacturing. Furthermore, the report called for Europe to draw lessons from other regions and focus resources on a single large-scale leader in advanced chips, supported by a clear strategic focus and strong public–private alignment. ([24])

The Competitiveness Compass ([25]), a roadmap to restore Europe's economic dynamism and boost growth, was the Union's first response to Prof. Draghi's call to address the key challenges identified in his analysis: closing the innovation gap with the US and China, harmonising decarbonisation with competitiveness, and enhancing economic security by reducing dependencies.

([20]) The related policy measures are subject to the ongoing interinstitutional negotiations related to the Multiannual Financial Framework.
([21]) Mario Draghi. (2024). The future of European competitiveness: In-depth analysis and recommendations (Part B).
([22]) Priorities 2024-2029 - European Commission
([23]) **Finishing processes** refer to the back-end stages of semiconductor manufacturing, encompassing assembly, packaging, and testing operations that transform processed wafers into functional, market-ready devices. Advanced finishing techniques such as 2.5D/3D packaging and chiplet integration are increasingly critical to semiconductor performance and represent a growing source of competitive differentiation in the global value chain.
([24]) The Draghi report: one year on
([25]) Competitiveness compass - European Commission

Several initiatives and measures in the Competitiveness Compass are of direct relevance to the strategic development of the EU's semiconductor industry. For example, the upcoming Cloud and AI Development Act will include **actions in relation to cutting-edge AI chips** through the stimulation of new data centres in the EU and can be a source of demand generation that will support the aims and objectives of the revised Chips Act. The **AI Continent Action Plan Communication** ([26]) outlined how, as part of the broader effort to develop **AI Gigafactories**, the Union aims to realise "***strategic autonomy in the design and production of AI semiconductors, reduce dependencies on critical technologies,*** *and* ***strengthen sovereignty in cutting edge semiconductors".*** It consequently called for the acceleration of preparatory work towards a revised Chips Act in 2026.

The **Industrial Action Plan for the European automotive sector** ([27]) underscored the importance of the semiconductor industry for an innovative and digitalised automotive sector. The transition to Software-Defined Vehicles, in which semiconductors will serve as a central and differentiating element, further highlights the need for a robust and competitive semiconductor ecosystem in the EU.

This initiative is also linked to the **Joint Communication on Strengthening Economic Security** ([28]), which underlines that access to high-quality information and its thorough analysis are the foundation of effective, well-informed EU economic security policymaking and decision-making. In this context, this initiative contributes to strengthening supply chain resilience and reducing strategic dependencies, while developing and maintaining EU leadership in critical technologies. Similarly, the initiative is coherent with the adopted **EU Action Plan on Drone and Counter Drone Security**, in particular with the aim to the development of a competitive European drone market.

Chips Act 2.0 is also designed in complementarity with other initiatives such as the Important Projects of Common European Interest (IPCEI). Here, the preparation of the upcoming IPCEI on Advanced Semiconductor Technologies (AST) ([29]) is a welcome initiative and fully in line with the spirit of the **Chips Act** by addressing the crucial bridging of the lab-to-fab gap.

Chips Act 2.0 is designed to be compatible with the current MFF (2021-2027) and the next MFF (2028-2034), including the European Competitiveness Fund and Framework Programme 10 (FP10). Its architecture will allow for immediate action and impact under the current MFF while ensuring continuity and scalability under the next MFF. The proposal does not alter or circumvent the design and architecture set out in the Commission's proposal on the MFF 2028–2034, nor does it pre-empt its implementation.

([26]) The AI Continent Action Plan | Shaping Europe's digital future
([27]) Action plan on the future of the automotive sector - Mobility and Transport
([28]) Commission announces strategic approach to strengthen Europe's economic security
([29]) The IPCEI AST is designed to build on existing EU initiatives, in particular pilot lines and the EU Chips Design Platform, ensuring continuity and acceleration rather than duplication. Driven by megatrends such as AI, automation, security and sustainability, IPCEI AST should provide a collective European response to disruptive technological change. It focuses on key technology areas including AI chips and accelerators, photonic integrated circuits, heterogeneous integration and advanced packaging, sensors, power electronics, energy-efficient solutions and secure communication, while covering the full semiconductor value chain, including enabling technologies such as EDA, equipment, testing, materials and wafers.

Furthermore, the revised options under Chips Act 2.0 are designed to remain coherent with existing State aid and competition frameworks, in particular the R&D&I Framework and the IPCEI Communication, while preserving their distinct objectives. As under the current framework, the IPCEIs and the R&D&I Framework will continue playing a central role in supporting research, development, innovation and first industrial deployment, notably for highly innovative and cross-border projects with strong spillover effects.

Measures under Chips Act 2.0 will build on this architecture by further clarifying and refining the scope of the First-of-a-Kind (FOAK) framework under Pillar II, which addresses a complementary and previously insufficiently covered investment gap at the manufacturing stage.

Chips Act 2.0 will also be coherent with the Chips Joint Undertaking (JU), established under Council Regulation (EU) 2021/2085 ('Single Basic Act') and funded by the **Digital Europe** and the **Horizon Europe** programmes, given that it is the main body responsible for implementing four of the five Pillar I objectives of the current and the revised Chips Act, i.e., pilot lines, the design platform, competence centres, and quantum chips.

Finally, Chips Act 2.0 is consistent with European cybersecurity legislation. Certain categories of chips are in scope of the **Cyber Resilience Act** and investments under the Chips Act will aim to complement its objectives by building on the strength of the European industry in the secure chips market segment.

Cybersecurity risks, including risks related to dependency on high-risk suppliers, may be observed in several critical Information and Communication Technologies (ICT) supply chains in the Union, including semiconductors. The recently adopted proposal for the revision of the **Cybersecurity Act** puts in place supply chain security requirements for certain sectors based on both "technical" and "non-technical" criteria. This would allow to exclude high-risk suppliers from third countries posing cybersecurity concerns from tendering for certain critical infrastructures in the EU, thus potentially increasing the demand for chips from domestic undertakings or undertakings from third countries providing equivalent assurances. In turn, **Chips Act 2.0** will support EU semiconductor manufacturers to invest in order to increase their production and maintain their leading position in secure products to be able to fulfil this demand, and add a security of supply dimension for the semiconductors publicly procured by critical entities. In concert with this approach, the Communication on Technological Sovereignty accompanying the Chips Act 2.0 proposal will announce that a cybersecurity risk assessment will evaluate both technical vulnerabilities and non-technical factors in anticipation of the revision of the Cybersecurity Act.

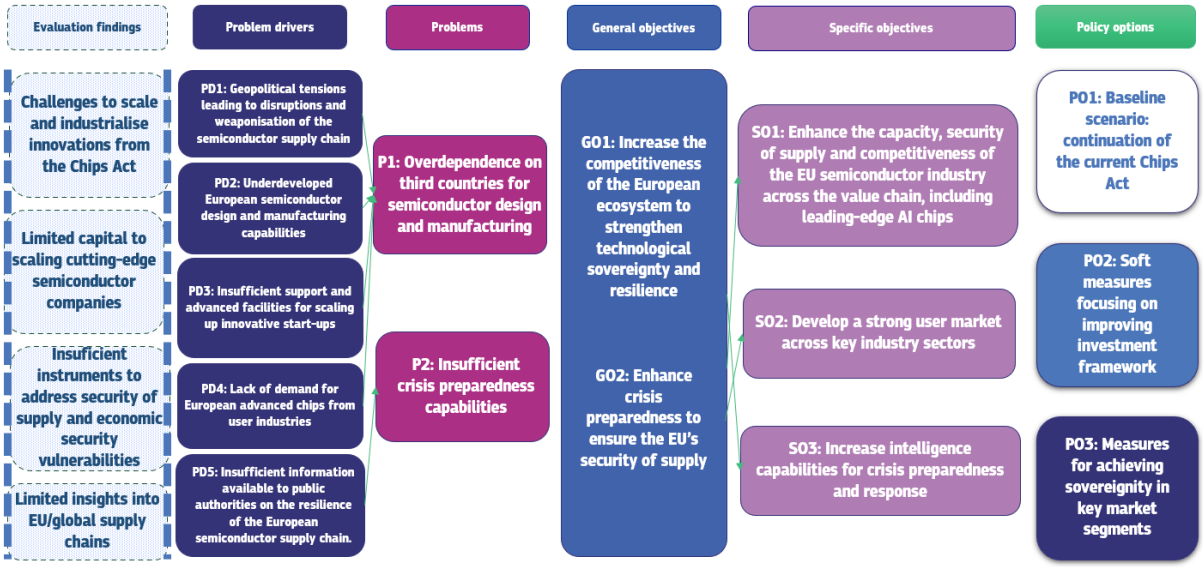

Figure 1- Intervention logic

2 PROBLEM DEFINITION

2.1 What is/are the problems?

The semiconductor value chain is critical to a wide range of industrial sectors. Its complexity makes it inherently fragile, and the Union's industry has experienced significant supply disruptions in recent years, which prompted the adoption of the first Chips Act on the 13 of September 2023. Despite those efforts, the EU continues to face major challenges in ensuring the secure, resilient and reliable supply of critical semiconductors. In this context, the two key problems that the revision of the Chips Act aims to resolve are the following: (1) overdependence on third countries for semiconductor design and manufacturing and (2) insufficient crisis preparedness capabilities.

2.1.1 P1: Overdependence on third countries for semiconductor design and manufacturing

The EU's semiconductor ecosystem **lacks sufficient design and manufacturing capacity to support its industrial base and wider digitalisation efforts. It is too reliant on a small number of countries and external actors.** Given the pervasiveness of semiconductors, this problem has a Union-wide dimension and carries important implications for all Member States.

Semiconductor shortages are a lived experience for industry in the EU. Supply shortages resulting from the COVID-19 pandemic cost the European automotive sector over EUR 100 billion from 2021 to 2022([30]), and the recent Nexperia disruptions ([31]) resulted in an estimated

([30]) Missing chips cost EUR100bn to the European auto sector | Allianz
([31]) Europe's carmakers face 'devastating' chip crisis as Nexperia supply crunch continues Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl

EUR 5 billion in lost output ([32]). Around 40% of the end-user participants in the open public consultation (OPC) reported chip shortages over the previous 12-24 months and a majority expect supply disruptions in the next 2-3 years, underlining how supply disruptions are becoming a lived experience for European industry ([33]). Workshop participants as well as interview partners also observed overdependence on Asian suppliers, in particular when it comes to high-performance chips. Examples provided by stakeholders in the medical, industrial and telecoms sectors illustrated the resulting vulnerability of Europe's supply chains ([34]).

Disruptions at Nexperia

On 30 September 2025, the Dutch Minister of Economic Affairs issued an order ([35]) under its national Goods Availability Act regarding the semiconductor manufacturer Nexperia. ([36]) Separately, on 1 October 2025, the Amsterdam Enterprise Chamber of Appeal took interim measures related to the company. ([37]) Shortly afterwards, the Chinese authorities imposed company-specific export control measures on all Nexperia locations in China. This prevented packaged chips manufactured by Nexperia in China, following front-end production in Europe, from being re-imported into the EU. Economic operators in the EU and elsewhere faced shipment delays and stoppages, with knock-on effects for downstream industries and resulting production disruptions. Automotive manufacturers warned of potential production halts. ([38]) The Chinese government eased export restrictions in early November and shipments of available chips have resumed, but uncertainties remain, and dwindling stocks may lead to further production disruptions in a multitude of end-user industries, including the automotive sector. ([39])

2.1.1.1 Market concentration and clustering in the semiconductor industry

The semiconductor supply chain is prone to disruption due to the strong concentration of semiconductor manufacturing at both regional and company level. According to the Organisation for Economic Co-operation and Development (OECD)[40], in 2025, China, Taiwan, South Korea, Japan, and the United States accounted for 87% of global in-production wafer capacity, while the ten largest manufacturers held about half of the total global capacity. This concentration has structurally increased but is a result of cumulative processes that ran over decades[41]. Several factors have contributed to this situation.

First, a big part of the technological knowledge in the semiconductor domain is process knowledge, which has been accumulated by companies over years and cannot easily be acquired by another firm, since it is bound to human capital and subject to strict intellectual

([32]) Europe's Carmakers Brace for Severe Chip Supply Crisis
([33]) Annex 2 Sections 4, 5 and 6.
([34]) Annex 2 Sections 4, 5 and 6.
([35]) Pursuant to the order, the Dutch Minister of Economic Affairs may block or reverse company decisions where they are, or could be, harmful to the company's interests, its future as a Dutch and European enterprise, and/or the preservation of this critical value chain for Europe.
([36]) Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl
([37]) ECLI:NL:GHAMS:2025:2752, Gerechtshof Amsterdam, 200.359.769/01 OK 2
([38]) Automotive alarm: "Without Nexperia chips imminent stop in production." EU mediates betwe…
([39]) Honda to halt production at plants in Japan and China due to chip shortage - The Japan Times
([40]) The chip landscape. Geographical distribution of wafer fabrication capacity
([41]) The chip landscape. Geographical distribution of wafer fabrication capacity; Semiconductors and Modern Industrial Policy

property protection and trade secrets. This cumulativeness of the knowledge base gives incumbent firms a significant head start.

Second, manufacturing is characterised by very high upfront CAPEX costs, which can go up to USD 20 to 30 billion for a leading-edge fab. This makes it very difficult for new companies to enter the market and is a powerful force for market consolidation. High fixed costs require consistently high utilisation rates in order to ensure economically viable production, creating strong economies of scale which further contribute to market concentration. In addition, customer relationships in the sector are highly entrenched, making it difficult to enter new market segments or attract customers as illustrated by the challenges faced by Intel in entering the foundry market ([42]).

Finally, semiconductor firms crucially depend on a dense local ecosystem of specialised suppliers and service firms. Key manufacturers are surrounded by a web of specialised suppliers, chemical providers, equipment servicers, and a deep pool of trained engineers.

2.1.1.2 Semiconductor dependencies in the EU

In 2024, total chip consumption in the EU reached EUR 55 billion, of which EUR 43.6 billion was imported from third countries ([43]). **EU-based production** therefore **accounts for only 22% of the Union's overall chip consumption** ([44]). Out of EUR 43.6 billion in semiconductor imports in 2024, 35% originated from China and Taiwan as seen in **Figure 3**.

It is important to note that these figures largely reflect the final stages of the value chain and may underestimate upstream stages (including some in the EU), given that many dies are only packaged in these countries at the final stage of chip production. Moreover, the data does not capture chips imported as part of finished systems.

([42]) See Evaluation of the Chips Act
([43]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.
([44]) Excluding chips imported as part of broader systems; Decision Etudes & Conseil and YOLE Group, Addressing dependencies under Chips Act 2.0, Nov.2025.

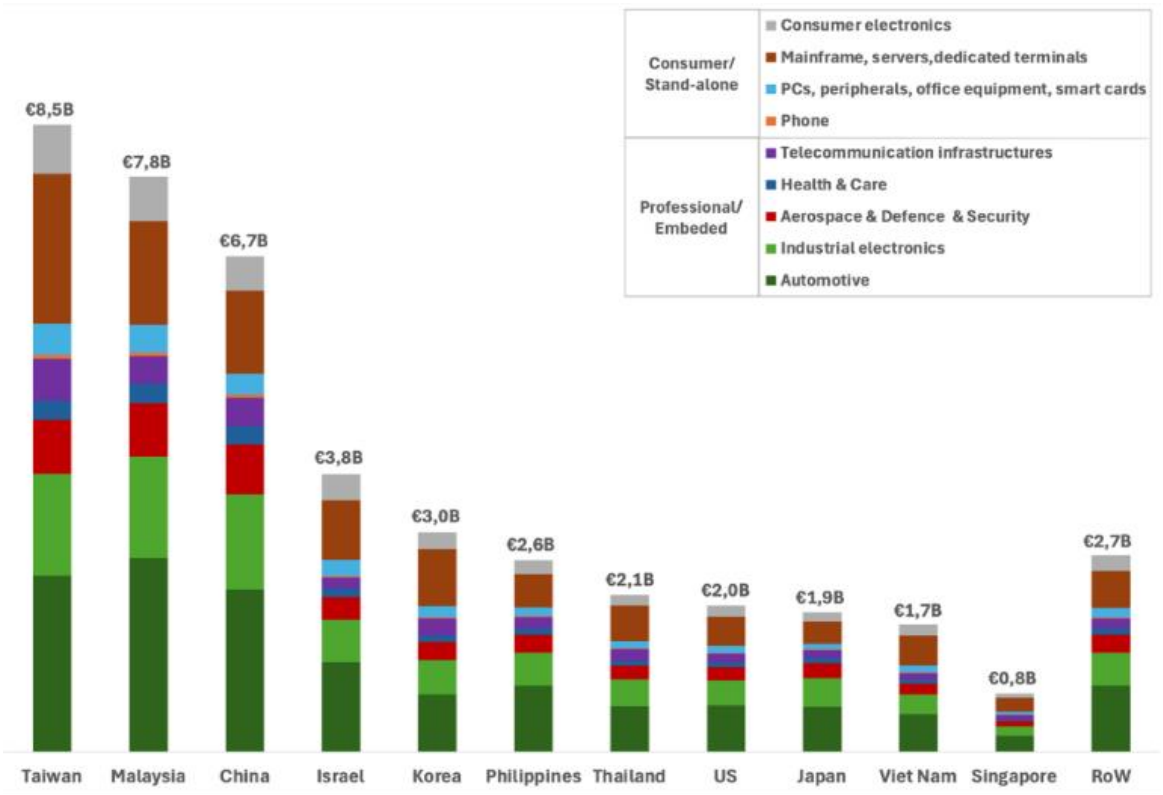

Figure 3 - EU chips consumption by origin of supply, 2024 (EUR Billion) (Source: Yole/Decision)[45]

For the purposes of this Impact Assessment, four key areas of overdependence will be analysed: first, in the design and manufacturing of leading-edge chips, which are critical to a competitive and resilient AI value chain in the EU; second, in mature-technology chips, which remain essential to industries such as automotive and industrial automation; third, in memory chips; and finally, across upstream stages of the semiconductor value chain from a broader perspective.

[45] Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

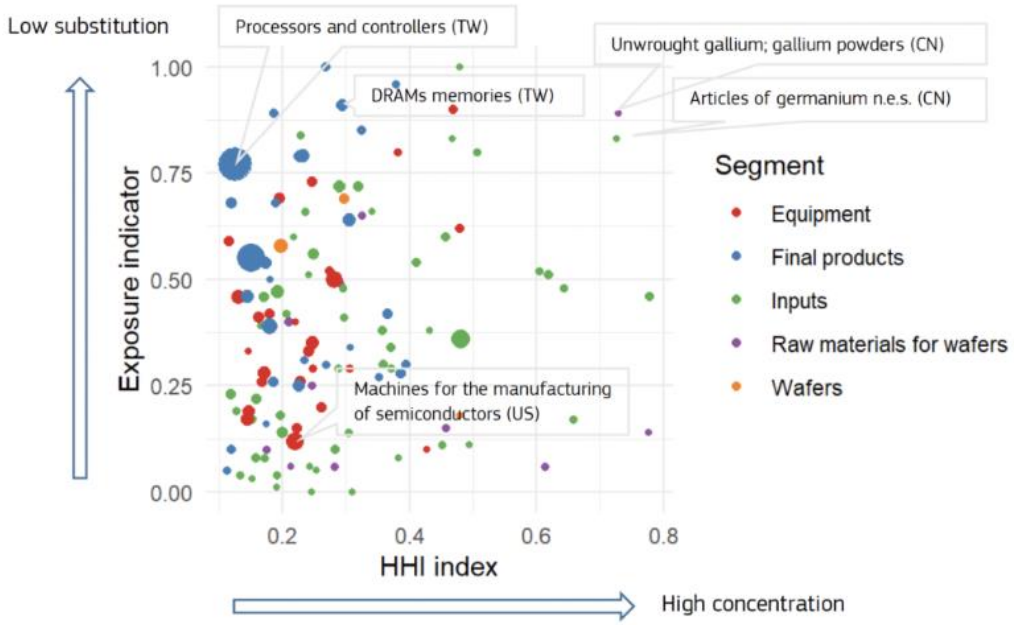

Figure 4 - Concentration of imports and potential substitution with EU production, by product, 2023 (size of bubble denotes import volumes) (JRC, 2025).

As seen **in Figure 4**, which provides a general overview of Europe's exposure along the semiconductor value chain, certain strategic inputs for the industry are acute EU supply vulnerabilities. Products such as unprocessed gallium and germanium have minimal EU domestic production and depend heavily on imports from China, creating concentrated single-source exposure even where total import values are modest. Similar dependency risks appear in several semiconductor categories: DRAM memories and specific processor/controller subsegments show limited scope for domestic substitution, while large import volumes are sourced primarily from Asian suppliers, notably Taiwan. This combination of high import concentration and low substitutability heightens the EU's vulnerability to geopolitical shocks, export controls, and supply chain disruptions. **These dependencies are further analysed in this sub-section, subsequent problem drivers and in Annex 4.**

2.1.1.3 Leading-edge chips

The Union's overdependence is most striking when it comes to leading-edge and advanced chips used for AI, high-performance computing, defence, or telecom applications ([46]). As of today, **the EU has no foundry capacity for leading-edge semiconductor manufacturing** and is fully dependent on chip designs originating in the US and on fabrication capacities located in Taiwan and South Korea ([47]). In Leixlip, Ireland, one can find leading-edge

([46]) Leading-edge and advanced chips are produced at very small node sizes (currently at 7nm to 3nm, with 2nm being ramped up).
([47]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

capacity (Intel 3 i.e. 3nm, one generation behind the current state-of-the-art) estimated at around 35,000 300mm wspm (wafer starts per month) that is used for Intel's own internal manufacturing, as part of its Integrated Device Manufacturer (IDM) model. ([48])

Furthermore, capacities for the **design of leading-edge chips** leading to mass manufacturing are virtually non-existent in the EU ([49]). Design is an important part of the problem, since production facilities need demand for the economic viability of manufacturing leading-edge chips. Europe faces a chicken-and-egg problem, as one weakness contributes to another vulnerability. Despite over EUR 80 billion in announced investments stemming from the Chips Act, the EU still lacks a full-fledged open foundry with capacities to produce chips below 10nm ([50]).

In the absence of AI chips designed and manufactured in the Union, Europe's dependence on this rapidly expanding market segment is increasing at an alarming pace. As cutting-edge chips underpin virtually all future strategic growth markets, ranging from defence and security to drones, humanoids and service robotics, autonomous vehicles, and 5G/6G networks, there is a significant risk that Europe will be excluded from the future growth markets that will define economic competitiveness and technological sovereignty ([51]).

2.1.1.4 Mature node chips

Mature node chips are chips fabricated with older generation, well-established manufacturing processes, larger in node size. Their reliability and cost-effectiveness make them widely used in various applications where cutting-edge performance is not necessary.

European semiconductor companies have long-standing strengths in microcontrollers (MCU), analogue, sensors and power devices. In these segments, EU consumption is high, and front-end capacity is well aligned with the needs of EU industries: MCUs and analogue chips which benefit from a robust 40–90 nm production in the EU; Micro-Electro-Mechanical Systems (MEMS) that build on established EU competencies; and power electronics, where the EU benefits from a strong base of device manufacturers, particularly in the rapidly growing Silicon Carbide (SiC) segment.

However, as node sizes go smaller than 40nm, supply chain vulnerabilities start to emerge. Investments stemming from the Chips Act, particularly the ESMC project in Dresden,

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In 2023, foundry manufacturing capacity at technology nodes of 7 nm and below was highly concentrated, with Taiwan accounting for 77% and South Korea for the remaining 23%. Intel's manufacturing capacity in Leixlip, Ireland is intended for internal use as discussed above. In 2024, 96% of AI chips sold in the EU were from US vendors (source: Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.).

([48]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report; The Intel Leixlip fab also has foundry capacity at 16nm.

([49]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

([50]) Intel exit in Magdeburg: "This is not a good day for Europe" | heise online

([51]) McKinsey technology trends outlook 2025 | McKinsey

Germany, should improve the situation, with upcoming capacity in 28/22nm technology and eventually 16/12nm.[52]

The European industry in the mature node segment is also threatened from the ramping up of capacity in Asia, leading to possible overcapacity risks in certain sectors. For instance, China's massive capital expenditure has outpaced all other regions, rising from 6.8% of global CAPEX in 2012 to 42.3% in 2024, 36.5% in 2025 and 31.5% in 2026 (until April '26).

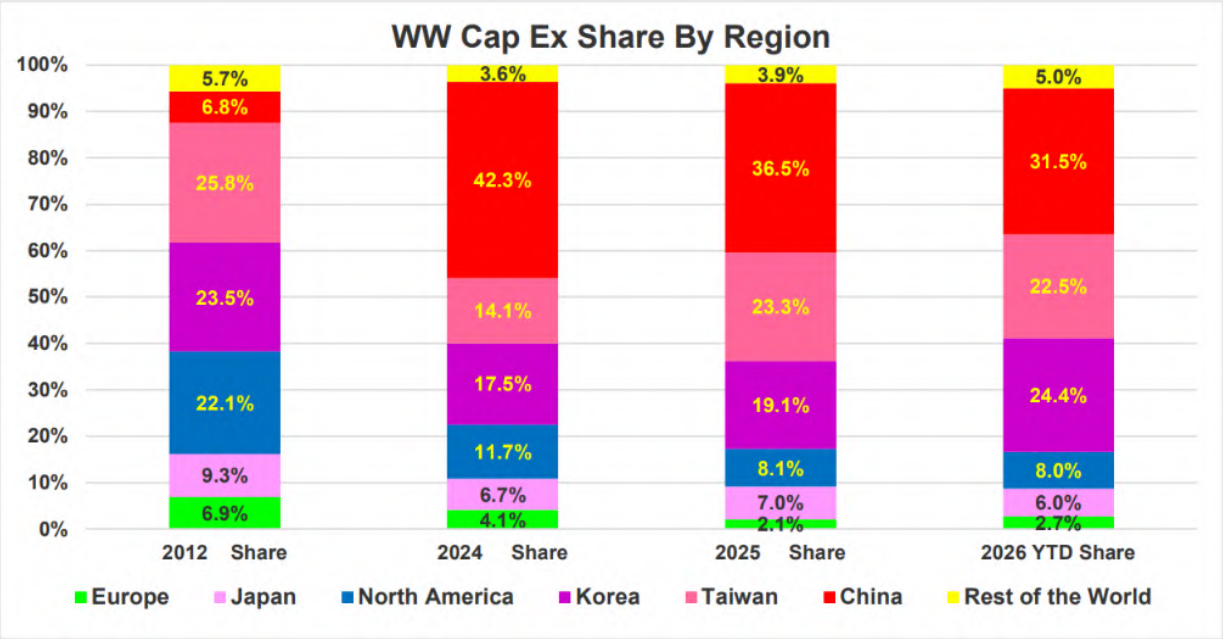

Figure 5 - Worldwide CapEx spend by region (Source: Future Horizons 2026)[53]

A key vulnerability can also be found in back-end processes where the EU semiconductor industry relies on imports from key back-end manufacturing hubs such as China, Taiwan and Southeast Asian countries ([54]). In fact, packaging and testing of mature node semiconductors are largely performed in Asia ([55]). When it comes to power SiC devices, module packaging and assembly for power devices are often done outside the EU with additional exposure to non-EU sourced substrates and epitaxy. With regards to MEMS the packaging/test step is also frequently done in third countries. This reality creates significant operational risks in crisis situations and may weaken supply assurance for European OEMs, even when front-end manufacturing is located in the EU, as exemplified by the Nexperia case presented above.

([52]) Commission approves €5 billion German State aid measure to support ESMC in setting up a new semiconductor manufacturing facility | Shaping Europe's digital future

([53]) Future Horizons, The Global Semiconductor Monthly Report, April 2026.

([54]) China and Taiwan account for 58.2% of OSAT facilities and South East Asian countries for a further 12.5% Source SEMI/TechSearch International Worldwide Assembly & Test Facility Database 2025

([55]) None of the Top 20 Outsourced Semiconductor Assembly and Test (OSAT) companies in terms of revenue are headquartered in the EU. Source: SEMI/TechSearch International Worldwide Assembly & Test Facility Database 2025.

2.1.1.5 Memory chips

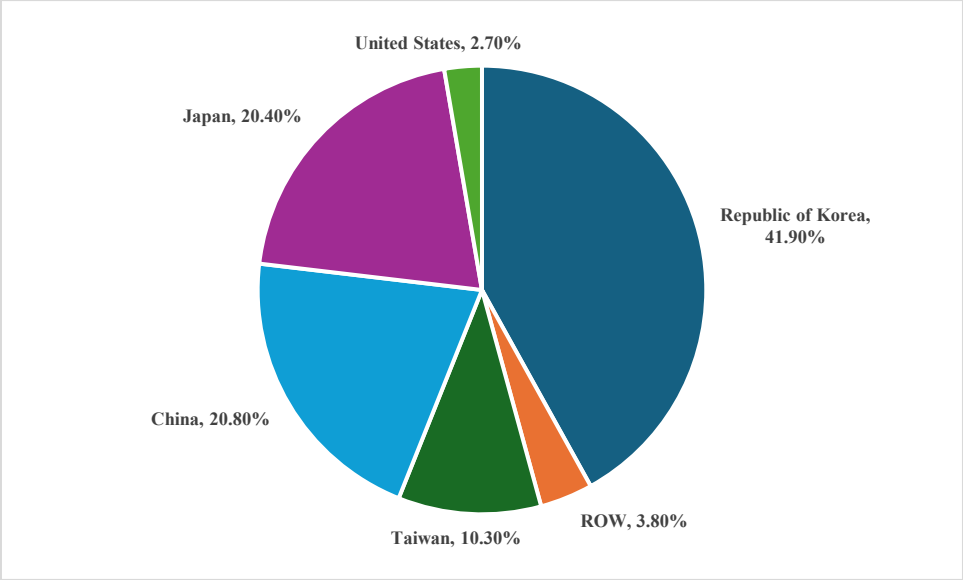

Figure 6- Memory manufacturing capacity by region in 2023 (Source: IDC)[56]

Europe has no significant manufacturing capacity in memory technologies, as shown in **Figure 6**. This is a key vulnerability in light of the criticality of memory chips, particularly DRAM and HBM for AI applications.

As shown in **Figure 7,** the memory market for both DRAM and HBM is dominated by three key manufacturers: SK Hynix (South Korea), Samsung (South Korea), and Micron (United States). In the DRAM market, ChangXin Memory Technologies (CXMT) (China) is emerging as a significant player, whereas the EU has no player in this market.

In fact, South Korea, China and Japan hold 83.1% of all manufacturing capacity, with South Korea being the dominant player in this segment due to the presence of SK Hynix and Samsung.

[56] IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report. Risks here include economic downturns or market turbulations.

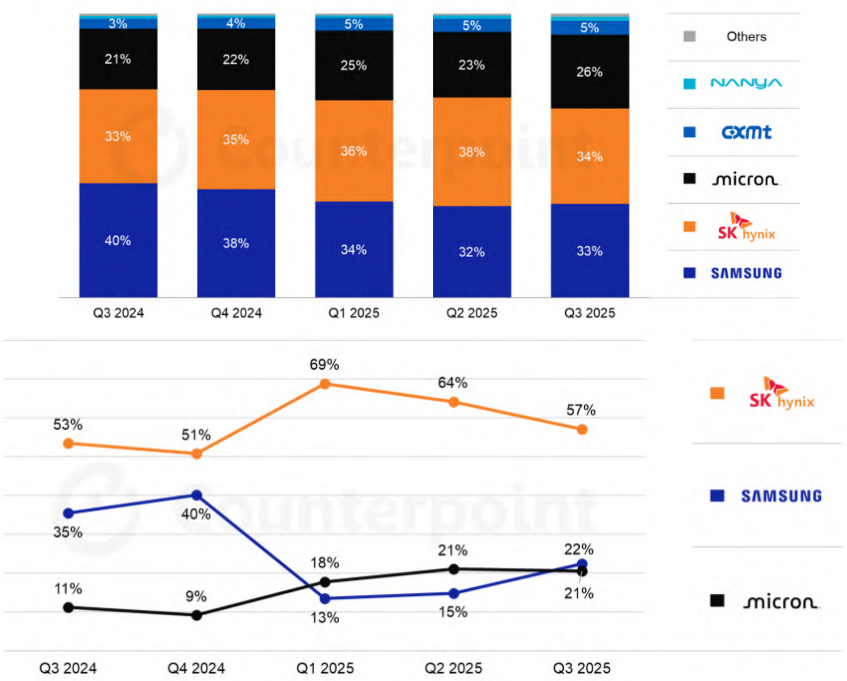

Figure 7- Global DRAM (top) and HBM (bottom) market share Q3 2024 - Q3 2025 (Source: Counterpoint)([57])

As of 2025, the semiconductor supply chain is grappling with a severe memory-chip shortage, with downstream impacts on device makers and consumers in terms of costs and security of supply. In particular, DRAM costs have risen steeply as AI data-centre demand keeps exceeding available supply, deepening the market imbalance.

DRAM						
Discrete products	60	59	58	59	64	72
High-bandwidth memory	58	57	56	57	60	66
NAND						
Discrete products	85	80	78	80	82	84
Solid state drive	82	76	75	77	79	81

Table 1 - Share of memory demand met by current supply (%) (Source: IBS)[58]

Demand for **high-bandwidth memory (HBM)** is rising sharply alongside AI server deployments, while supply growth is constrained by concentrated manufacturing capacity and

([57]) Global DRAM and HBM Market Share: Quarterly
([58]) IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

long build-and-qualification lead times ([59]). Manufacturers are prioritising higher-margin HBM and server-grade DRAM output, tightening availability for more commoditised DRAM and lifting pricing across adjacent segments ([60]). This is compounded by limited advanced packaging and stacking capacity required for HBM, which implies that additional wafer starts do not translate quickly into shippable volume.

Demand for NAND used in discrete products and solid-state drives in data centre applications is also rising faster than available supply. Market analysts conclude that significantly expanding NAND capacity is challenging, as most wafer fabrication facilities are already operating near full utilisation ([61]).

As seen in **Table 1**, fab capacity for both DRAM and NAND, none of which is in Europe, is well below demand. This is expected to persist until at least 2027 and may end up delaying the deployment of AI infrastructure and data centres.

2.1.1.6 Upstream value chain segments

As further elaborated on in Annex 4, the Union remains exposed to persistent risks of semiconductor supply chain disruptions, while significant overdependencies are also evident in other segments of the value chain. In fact, the semiconductor industry relies on a complex network of suppliers providing inputs to each other across the value chain, from Electronic Design Automation (EDA) software, to materials, to manufacturing equipment.

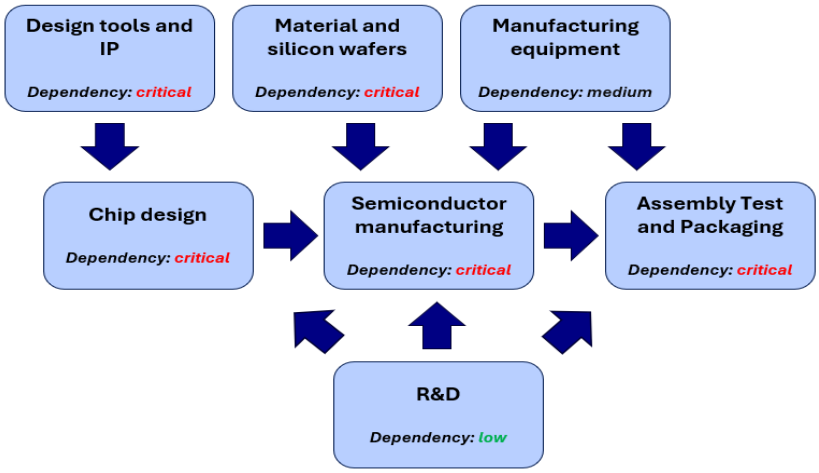

Figure 8 - European dependencies along the semiconductor value chain (see Annex 4)

2.1.1.6.1 Electronic Design Automation

EDA tools are essential for designing integrated circuits and the market is highly concentrated: Synopsys (US), Cadence (US) and Siemens EDA (EU-headquartered)

([59]) AI's memory chip champion has a value problem | Reuters
([60]) https://www.trendforce.com/presscenter/news/20251029-12758.html
([61]) IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

accounted for over 75% of global share in 2024, rising to around 80% after Synopsys's 2025 acquisition of Ansys. EDA software is delivered as an interoperable suite spanning the full, iterative design flow (front-end verification, synthesis, physical implementation, and sign-off), making substitution difficult. The remaining market share is largely from Empyrean (China), which mainly serves domestic customers and is not a credible alternative for European industry, while smaller vendors and open-source solutions lack complete, reliable, foundry verified, end-to-end leading-edge toolchains. Europe's position is also constrained since Siemens EDA largely offers US-origin intellectual property deriving from the acquisition of Mentor Graphics, and is therefore potentially exposed to US export controls, while Synopsys and Cadence retain key advantages in hard-to-replace advanced-node tools, further reinforced by Synopsys' expanded multiphysics simulation via the Ansys acquisition.

This US-jurisdiction concentration creates geopolitical leverage, underscored for example by the Bureau of Industry and Security's (BIS) licensing requirements introduced in May 2025 for EDA tool provision to Chinese customers. A hypothetical comparable restriction against Europe would severely limit Europe's ability to design advanced chips.

2.1.1.6.2 Materials

2.1.1.6.2.1 Critical raw materials

Semiconductor manufacturing draws on materials across much of the periodic table, from relatively abundant silicon to rare earth elements. ZVEI analysis([62]) indicates that the number of elements used in the semiconductor industry has quadrupled over the past thirty years (**Figure 9**), increasing exposure to concentrated supply chains for certain critical inputs.

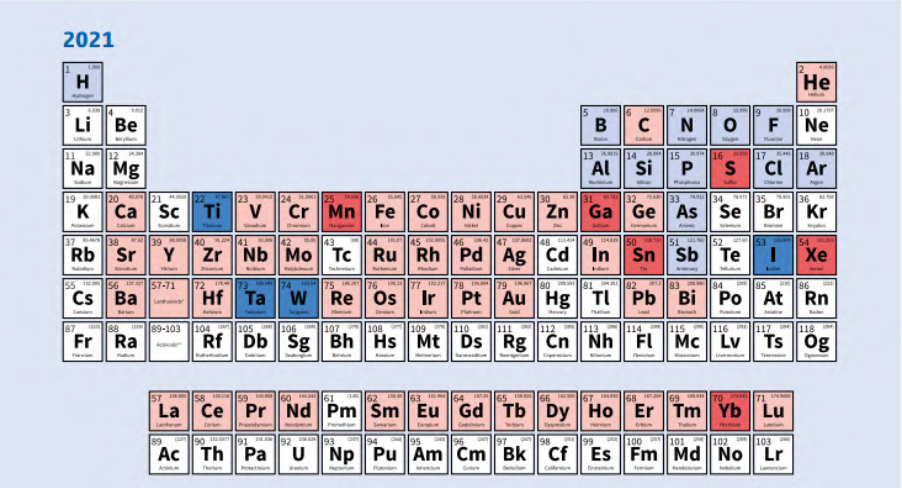

Figure 9 - Elements used in the semiconductor industry, where coloured elements denote use (Source: ZVEI)

Key examples here include gallium (Ga) and germanium (Ge)..The Union is heavily reliant on China for gallium for use in integrated circuits (around 70%), with the remainder primarily

([62]) Semiconductor-Strategy-for-Germany-and-Europe | ZVEI Light blue indicates elements in use in the 1980s; Dark blue indicates elements in use in the 1990s; Light red indicates elements in use in the 2000s; Dark red indicates elements in use in the 2010s.

in LEDs (around 25%) and photovoltaics. ([63]) Use in power electronics is increasing. Germanium production is also concentrated in China (around 79%), followed by the United States (around 16%) and the United Kingdom (around 3%). EU demand is mainly for infrared optics (around 52%), optical fibres (around 23%) and satellite solar cells (around 12%).([64]) Diversification appears comparatively more feasible for germanium than for gallium.
Gallium enables key compound semiconductors for RF, power and optoelectronics (e.g., GaAs for high-frequency RF devices and GaN for high-power and high-voltage applications), while germanium is relevant for SiGe RF devices and silicon photonics, and features in leading-edge transistor integration.

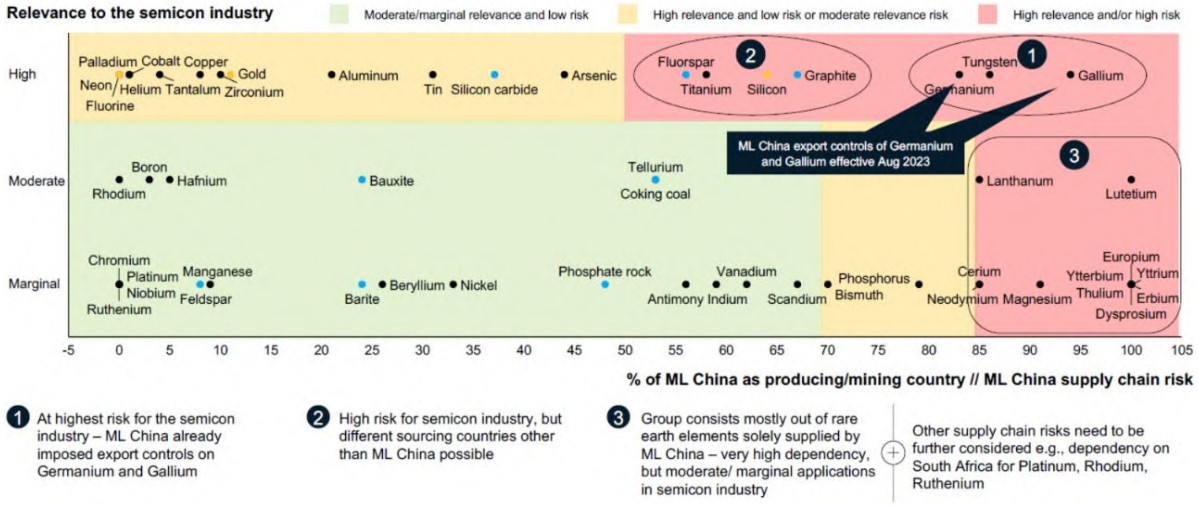

Figure 10 - Critical raw materials in the semiconductor industry (Source: McKinsey)

The examples of gallium and germanium are crucial since, as seen in **Figure 10**, Chinese dominance over these materials has allowed for the introduction of disruptive export controls on gallium and germanium (and related compounds) from 1 August 2023 ([65]), requiring exporters to obtain licences. The measure is widely understood as part of ongoing geopolitical rivalries and trade confrontation and is viewed as a response to the tightening of restrictions on China's access to advanced semiconductor manufacturing equipment and know-how, including lithography-related controls. These export controls have resulted in prices for these raw materials to increase by around 20% ([66]).

2.1.1.6.2.2 Compound semiconductor substrates/epiwafers

A compound semiconductor substrate is a high-purity crystalline wafer (typically SiC, GaAs or InP) that provides the mechanical base and lattice structure for compound devices and the epitaxial layers grown on top, enabling applications such as RF, power electronics and photonics. The substrate supply chain is highly concentrated and regionally segmented, with suppliers specialising by material platform; Yole Intelligence indicates Europe's merchant footprint is relatively narrow (notably Freiberger Compound Materials for GaAs and InP),

([63]) SCRREEN2_factsheets_GALLIIUM.pdf
([64]) SCRREEN2_factsheets_GERMANIUM-1.pdf
([65]) Yole Group, Status of the Compound Semiconductor Industry 2024.
([66]) Yole Group, Status of the Compound Semiconductor Industry 2024.

while substantial global capacity sits in the United States and East Asia (including Japan, China and Taiwan) ([67]). Europe's exposure is partly mitigated in SiC by increasing vertical integration: STMicroelectronics is developing in-house SiC substrates in Catania under its "Silicon Carbide Campus" (supported by an Italian Chips Act-aligned State-aid measure)([68]) and Onsemi is expanding SiC-related capacity in Rožnov (backed by a Czech Chips Act-aligned State aid measure),([69]) building capability inside integrated manufacturers even as the merchant base remains limited.

Immediately downstream, epiwafers add performance-critical epitaxial layers (e.g. SiC, GaAs, InP, GaN-on-SiC). Epitaxy is process-sensitive and qualification-heavy, making switching slow and costly. Yole mapping suggests the EU's identifiable merchant epiwafer presence includes Soitec (France) and Azur Space (Germany), with much of global capability concentrated outside the EU, notably in Japan, Taiwan, the United States and China.([70])

2.1.1.6.3 Ultra-high-purity process gases and chemicals

2.1.1.6.3.1 Gases

Semiconductor manufacturing depends on ultra-high-purity process gases and precursors for deposition, etch, doping, chamber cleaning, surface treatments and lithography support. Since wafer fabrication is sequential and qualification-heavy, the loss of a single qualified molecule at the required purity can halt a process step and disrupt fab operations. Europe produces some standard, enabling gases (e.g., NH_3, Cl_2/HCl, N_2O/NO, SF_6 and certain hydrocarbons), but remains structurally dependent on external suppliers for many critical electronics specialty gases, especially those central to transistor formation and materials integration such as dopants (arsine, phosphine, diborane), key deposition precursors (silane/chlorosilanes, TEOS, germane, WF_6), and essential etch and clean chemistries (HF, HBr, NF_3, F_2/ClF_3 and fluorocarbons), with deuterium used in selected passivation/anneal steps. Upstream supply is also concentrated, with reports that over half of the EU's electronics specialty gas sources are heavily dependent on a single third country (China), amplifying disruption risk; if a critical externally sourced gas is constrained, tool uptime, cycle times and yields can deteriorate rapidly, with knock-on effects across the European value chain and downstream users.([71])

2.1.1.6.3.2 Chemicals

Semiconductor fabs rely on ultra-high-purity chemicals across all process steps (cleaning acids and bases, oxidisers, solvents, etch and deposition chemistries, and Chemical-Mechanical-Planarisation slurries), and these inputs are qualified to specific tools and recipes

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([67]) Yole Group, Status of the Compound Semiconductor Industry 2024.

([68]) STMicroelectronics to build integrated Silicon Carbide substrate manufacturing facility in Italy - STMicroelectronics

([69]) Commission approves €450 million Czech State aid for Onsemi's new semiconductor manufacturing facility

([70]) Yole Group, Status of the Compound Semiconductor Industry 2024

([71]) For semiconductor process gases, the applicable specification extends well beyond a nominal purity value (for example, 99.9999%). In practice, device manufacturers and equipment suppliers jointly qualify the gas as an integrated package, encompassing its detailed impurity profile, cylinder and valve materials, packaging configuration, and the performance of the associated delivery hardware. Any change in supplier, production site, or even cylinder type typically necessitates requalification, a process that can require several weeks to months and entails significant engineering effort and test-wafer consumption.

under strict purity specifications, so shortages or quality deviations can halt production and are not quickly solved by switching suppliers.

This section focuses on three illustrative chemicals: photoresists, polysilicon and deposition precursors. Photoresists are indispensable for Deep Ultraviolet (DUV) and Extreme Ultraviolet (EUV) lithography as the light-sensitive film enabling pattern transfer. In fact, they are co-developed and tightly qualified with fabs, making substitution slow and risky The supply base is also highly concentrated, with Japanese firms estimated at around 90% market share (notably JSR and TOK) ([72]), a vulnerability highlighted by the 2019 Japan–South Korea export licensing changes for certain semiconductor materials ([73]). High-purity polysilicon is the feedstock for silicon wafers: while photovoltaic-grade output is dominated by China, electronic-grade supply is more diversified with Germany's Wacker among leading suppliers alongside firms in the United States, Japan and South Korea. However, both segments depend on metallurgical-grade silicon, whose global supply is strongly China-dependent.

Finally, Atomic Layer Deposition (ALD) and Chemical Vapour Deposition (CVD) precursors are specialised molecules enabling atomic-scale deposition for advanced transistor and interconnect structures. The market was at EUR 1.7 billion in 2024 and is projected to exceed EUR 2.3 billion by 2028. In this segment, the EU holds a leading position through Merck (DE) and Air Liquide (FR), which together account for over half of global share in advanced precursors, although Chinese suppliers are scaling capacity.

2.1.1.6.4 Manufactured inputs

Manufactured inputs such as photomasks and advanced packaging materials are design-specific, tightly qualified and supplied by a small number of producers, so disruption can delay tape-out, constrain output and raise costs. Photomasks are fundamental inputs because each product and process node requires a dedicated mask set; supply is split between captive production (by leading foundries/IDMs) and the merchant market, with captive share rising from 35% to 65% between 2008 and 2020, leaving firms without in-house capability more exposed to tight merchant capacity during upcycles.([74]) Key merchant suppliers include Tekscend (JP), Dai Nippon Printing (JP), Photronics (US), SK-Electronics (JP) and Taiwan Mask Corporation (TW), with Tekscend also operating a Dresden facility supplying leading-edge masks (including EUV). Upstream concentration is even stronger in EUV mask blanks, where AGC (JP) and HOYA (JP) reportedly provide around 93% of supply, creating an additional bottleneck ([75]).

Advanced packaging has similar single-point risks. Nittobo's T-glass (low-Co-efficient of Thermal Expansion (CTE) glass cloth) used in package substrates to reduce warpage and support yield and reliability in large high-power packages (e.g., CPUs/AI/networking), is reported at approximately 90% market share. Ajinomoto's ABF dielectric film is reported at

([72]) Japan - Semiconductors profile - Trade.gov
([73])The South Korea-Japan Trade Dispute in Context: Semiconductor Manufacturing, Chemicals, and Concentrated Supply Chains
([74]) EUV mask technologies: evolution and ecosystem for devices
([75]) https://finance.yahoo.com/news/asml-holding-q4-earnings-investors-124600373.html?utm

around 95% market share and is essential for dense multilayer build-up substrates that connect advanced CPU/GPU dies to the wider system ([76]).

2.1.1.6.5 Manufacturing equipment

Chip manufacturing is highly equipment intensive. The equipment ecosystem is fragmented and specialised, with different tool families required for distinct process steps. For simplicity, this analysis distinguishes between **front-end manufacturing** and **back-end manufacturing**.

2.1.1.6.5.1 Front-end equipment

Front-end manufacturing (Front-end-of-line (FEOL) and Back-end-of-line (BEOL) wafer fabrication) covers the processes used to create semiconductor devices and interconnects on a silicon wafer, including transistor formation, deposition of dielectric and metal layers, lithographic patterning, etching, and planarisation.

In front-end equipment, Europe's most significant position is in **lithography**, where EU-based suppliers account for approximately **92%** of the market. This is a strong lever in a critical process step, but it is highly concentrated in a single segment and depends on coordination with the United States.
By contrast, the broader front-end wafer-fabrication equipment market is led by the **United States (~40%)**, followed by **Japan (~28%)** and **Korea (~24%)**, with the EU remaining in single digits. This indicates that Europe's influence over upstream manufacturing capacity is not commensurate with its strength in lithography. **Further analysis of the different segments of front-end equipment is provided in Annex 4.**

2.1.1.6.5.2 Back-end equipment

Back-end manufacturing (assembly, packaging and test) covers the final steps that convert processed wafers into finished, packaged devices ready for integration into electronic systems. It includes wafer dicing and thinning, die attach and interconnect, encapsulation (moulding and sealing), inspection and handling, and final electrical test. Packaging provides electrical connectivity for signals and power, supports heat dissipation, and protects the device to ensure long-term reliability.

The back-end equipment market is concentrated and increasingly dominated by Japan. In 2023, Japan accounted for **48%** of the global market (up from **33%** in 2017) and held a dominant position in dicing equipment (**>92%**). Japan also led packaging equipment overall (**51.4%**) and was particularly concentrated in moulding and sealing systems (**75.3%**). Singapore's share declined to **21%** (from **35%** in 2017), reflecting its specialisation in bonding equipment, especially wire bonding, where it accounted for **>81%** of global sales; Singapore also held **97%** of integrated assembly systems (with the remaining **3%** held by Grohmann Engineering, Germany). The EU held **14.5%** of the global market in 2023 (down from **16%** in 2017), with limited presence in several high-throughput segments but material

([76])https://www.nittobo.co.jp/eng/business/electronicmaterials/index.htm

positions in selected bonding and finishing categories. **Further analysis of the different segments of back-end equipment is provided in Annex 4.**

2.1.1.7 Conclusion

Across the semiconductor value chain, the Union remains exposed to material supply chain disruption risks and to persistent, structurally embedded dependencies on third country suppliers. In EDA, market concentration in US-jurisdiction providers and the limited substitutability of interoperable tool suites constrain the Union's strategic autonomy and create exposure to potential extraterritorial measures. In materials, vulnerabilities span upstream from critical raw materials with highly concentrated global production, through compound semiconductor substrates and epiwafers where merchant capacity is limited and regionally segmented, to ultra-high-purity gases and chemicals that are qualification-intensive and therefore difficult to substitute at short notice. While selected European strengths exist, they do not eliminate wider reliance on external supply bases for multiple process-critical inputs, including those relevant to lithography.

In manufactured inputs, design-specific and tightly qualified products such as photomasks and advanced packaging materials exhibit pronounced single-point failure risks, reinforced by high upstream concentration in certain enabling materials. In manufacturing equipment, the Union's strong position in lithography constitutes a strategic asset but is not matched by comparable capability across the broader front-end tool ecosystem, while back-end segments remain concentrated in non-EU suppliers. Overall, this configuration implies that a disruption or restriction affecting a limited number of concentrated upstream inputs can propagate rapidly across design, fabrication and packaging activities, with consequential impacts on European industrial capacity, downstream users and broader resilience objectives.

2.1.2 P2: Insufficient crisis preparedness capabilities

Since 2023, as will be elaborated on further in the problem drivers, geopolitical tensions have increased and several events have highlighted the vulnerability of the EU's semiconductor supply chain – including export controls on critical raw materials, the now withdrawn AI Diffusion Rules by the US ([77]) and the recent Nexperia case ([78]).

Despite the monitoring and crisis-response tools established under Pillar III of the Chips Act, significant gaps remain in the Union's ability to effectively address semiconductor supply chain crises. The EU still lacks sufficiently developed mechanisms, tools and institutional capacities to anticipate, assess and respond to disruptions in a timely and coordinated manner. Evidence gathered in the evaluation of the Chips Act ([79]) suggests that to capture system-wide risks, the scope of crisis response mechanisms needs to be extended to cover base materials,

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([77]) Federal Register: Framework for Artificial Intelligence Diffusion
([78]) Minister of Economic Affairs invokes Goods Availability Act | News item | Government.nl
([79]) During the evaluation, several interview partners and workshop participants considered the original design of the Chips Act with its focus on front-end fabrication to be misaligned with the current vulnerabilities, overlooking dependencies in substrates, specialty chemicals, advanced packaging, RF and power modules, PCBs and EMS (see page 48 and 49 of the Evaluation report).

substrates, materials, packaging, assembly, downstream electronics, and end-user industries. Not including these elements allows vulnerabilities in the value chain to go unnoticed, limiting the relevance of crisis response for downstream and end-user sectors, and eventually customers ([80]). Outside a formally activated crisis, the Union currently has no binding mechanism to gather information directly from undertakings, leaving the Commission without the means to assess ad hoc supply chain situations, identify emerging bottlenecks, or monitor dependencies in real time before they reach crisis activation thresholds.

The semiconductor value chain remains highly opaque and fragmented to public authorities, and the lack of device-level data makes it difficult to understand and predict global and European supply dynamics. **Pillar III's effectiveness is somewhat constrained by limited Union level visibility into Europe's semiconductor supply chains functioning and resilience of their operations**, thereby weakening crisis preparedness. Despite improved coordination through the European Semiconductor Board ([81]) and initial early warning measures, monitoring remains insufficiently integrated across value chain segments such as materials, equipment, design tools, and downstream users ([82]). Fragmented data sets restrict the Union's ability to anticipate disruptions, leaving initiatives under Pillar III with only partial system-level visibility.

Work under the European Economic Security Strategy ([83]) illustrates the limitations of the current system: as part of a risk assessment exercise ([84]), the Commission and Member States attempted to assess vulnerabilities in the supply of advanced semiconductor technologies and to gather data through surveys, workshops and interviews covering chip use, stock levels, suppliers, customers and user industries. However, the information collected by the Commission and Member States was limited since industrial stakeholders were not required to provide data on a mandatory basis. As a result, the joint risk assessment could not deliver the sufficiently detailed insight needed for a thorough understanding of the structure of the supply chain, or for the identification of critical dependencies and potential bottlenecks.

Given the global nature of semiconductor supply chains, no single Member State can obtain on its own the insights needed to assess risks or manage disruptions. Supply chains naturally involve cross-border dependencies, which means that national monitoring systems would be unable to address systemic EU risks creating potential blind spots and gaps in the data. Analysis of the Nexperia case has shown impacts in the automotive sector of several different Member States ([85]).

Overall, in the absence of enhanced monitoring capacities and crisis preparedness measures, the Union is unable to better anticipate disruptions, assess risks, coordinate responses and does not possess adequate tools to mitigate the impact of future crises.

([80]) Annex 2
([81]) Register of Commission expert groups and other similar entities
([82]) Annex 2
([83]) Press corner | European Commission – An EU approach to enhance economic security.
([84]) Communication on European economic security.pdf
([85]) Europe's carmakers face 'devastating' chip crisis as Nexperia supply crunch continues

2.2 What are the consequences?

The aforementioned challenges provoke considerable **economic costs that come from dependence and a lack of resilience.**

As the EU becomes increasingly reliant on foreign semiconductor supplies, it grows more vulnerable to external coercion and risks a potential 'weaponisation' of its supply chain dependencies. Without a strong industrial base in semiconductor design and manufacturing, the EU will not capitalise on its strong R&D ecosystem through productivity gains and the industrialisation of research.

User industries in the EU face significant uncertainties in their supply chains, leading to increased inventories and reduced investment which render manufacturing in the EU less competitive. Moreover, supply chain dependencies expose the EU to heightened geopolitical and security risks, particularly in crisis scenarios where access to critical technologies may be restricted or prioritised elsewhere. They may also affect the EU's autonomy in security and defence, with the defence industry unable to secure reliable access to vital electronic components, undermining long-term strategic autonomy and the credibility of EU policy commitments.

In summary, persistent dependence on non-EU semiconductor technologies constrains the EU's ability to exercise technological sovereignty, limiting its control over critical standards, architectures, and its ability to shape future innovation pathways. Even with the investments triggered by the Chips Act, critical gaps remain which hamper the development of crucial infrastructure such as AI datacentres.

2.3 What are the problem drivers?

The problems described above emerge from a mixture of external drivers, structural weaknesses of the European semiconductor sector, and the general framework for doing business in the EU which affect the competitiveness of the semiconductor industry.

2.3.1 PD1: Geopolitical tensions leading to disruptions and weaponisation of semiconductor supply chains

Amid rising geopolitical tensions, semiconductors have become a strategic technology, driving heightened global competition and prompting third countries to adopt increasingly aggressive industrial and trade policies across the semiconductor value chain and its end markets. While geopolitical tensions predate the adoption of the first Chips Act, a notable shift since its entry into force has been the sustained weaponisation of the supply chain. Furthermore, an escalation in hostilities can have an indirect impact on trade flows of semiconductors due to shocks on logistics.

As the semiconductor industry takes a more central role in economic security policy considerations worldwide, governments increasingly view secure access to semiconductors as a prerequisite for technological leadership, industrial competitiveness, national security and resilience. This shift has translated into a marked escalation in State intervention in the industry, which is now being felt more acutely since the adoption of various laws and subsidy schemes in all major semiconductor producing regions.

At the heart of the geopolitical dimension of the semiconductor industry is Taiwan that produces over 90% of the most **advanced logic semiconductors**, with its most prominent company TSMC being the leader in semiconductor foundry services, holding 67% of the global market share in Q4 2024.([86]) Taiwan is also an important source of mature-semiconductors, chip design and packaging.

Furthermore, rising frictions in the South China Sea over conflicting territorial claims also raise the risk of potential blockades and major disruptions. If a conflict were to materialise, this could result in a severe shortage of a broad range of semiconductors for EU companies, including the disruption or loss of access to advanced semiconductors such as AI chips and could lead to an estimated global GDP loss in the order of 10%. ([87])

Against this backdrop, the US, China, Japan and South Korea have each introduced substantial support schemes for the semiconductor industry, such as subsidy programmes and tax incentives, aimed at expanding domestic advanced manufacturing capacity and design. Both the US and China have implemented or explored restrictive trade measures, including export controls on advanced chips and related technologies. These policies indicate a broader move towards more state involvement in the management of semiconductor supply chains and reflect a growing recognition of their geopolitical and economic significance.

The absence of coordinated funding by the Union and Member States limits the possibility for EU-level policy steer of project selection, to align investments with identified European dependencies and ensure complementarity of investments. In a public consultation, interview partners and workshop participants also pointed to room for improvement in terms of coordination processes between the EU and national levels ([88]).

This subsidy race is drastically increasing manufacturing capacity worldwide, as Governments compete to attract new fabs and expand existing ones through massive public support packages. The result is a wave of capacity announcements that risks creating global overcapacities in mature and mainstream chips, intensifying price competition and further distorting the global level playing field, placing European semiconductor firms at a competitive disadvantage ([89]).

Furthermore, from a trade policy perspective, the ongoing geopolitical competition has resulted in disruptions to open, rules-based trade, which has been starkly felt by the semiconductor industry. The withdrawn US Framework for Artificial Intelligence Diffusion illustrate how technological dependency exposes the EU to supply chain vulnerabilities and risks of economic coercion. Such a policy would have consequently fragmented the internal market into Tier 1 and Tier 2 classes and resulted in certain Member States having constrained access to AI chips and systems ([90]). This illustrates how the weaponisation of

([88]) Annex 4.2 and 5.2
([89]) Beyond overcapacity: Chinese-style modernization and the clash of economic models | Merics
([90]) Joint Statement by Executive Vice-President Henna Virkkunen and Commissioner Maroš Šefčovič | European Commission

export controls as geopolitical tools can lead to concrete risks for security and competitiveness.

Conversely, recent restrictions from China on exports of gallium and germanium ([91]) risked undermining the production of vital power electronics components, RF and communications equipment and optoelectronic devices, which are also European strengths. The interruption in supply of electronic components from Nexperia has illustrated how in the current context, dependencies even in mature technologies can disrupt European user industries, particularly the automotive sector.

2.3.2 PD2: Underdeveloped European semiconductor design and manufacturing capabilities

Compared to the Union's share of global economic activity, the semiconductor industry in the EU remains underdeveloped in both design and manufacturing, limiting Europe's ability to compete in high-growth segments and increases its dependence on third countries for critical technologies.

When it comes to design, BCG–SIA estimates indicate that the design stage captures over 50% of total value-added in the semiconductor value chain. Yet, the EU **has a limited number of fabless companies** and none in the top 40 in terms of revenues, with the European market share being **less than 1%** ([92]). The EU commands only a very small share of the global design talent pool, with roughly 4% of the worldwide design workforce. This critical bottleneck in human capital severely limits the EU's ability to capture value in the highest-growth segments.

The EU's position is set to diminish further as the share of European design starts is projected to fall further by the end of the decade from 14.72% in 2018 to 11.75% in 2030 ([93]). Furthermore, chip design requires the use of tools and IP originating mostly from US companies. Consequently, European chipmakers rely on US-origin IP and software that are subject to export licenses whose terms are set by third countries. This critical dependency underscores the importance of Union-level action in the field of EDA and IP.

The Union's semiconductor industry is also shaped by the long-standing predominance of IDMs who design and manufacture chips, focusing mostly on analogue and mixed-signal chips, microcontrollers and custom logic in mainstream technology nodes. In fact, IDMs account for roughly 97% of the EU's semiconductor manufacturing revenue. Their vertically integrated model has historically aligned well with European end-markets, particularly automotive and industrial automation. However, this approach has its limitations and becomes unsustainable at more leading-edge technologies, explaining a global industry shift towards the fabless-foundry model, with firms specialising in either design or manufacturing due to

([91]) China gallium, germanium export curbs kick in; wait for permits starts | Reuters
([92]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.
([93]) IBS, Global Semiconductor Industry Service 2023 – Second in-depth analysis report.

high costs. This model has become the dominant configuration for advanced logic and high-performance chips.

Therefore, in a context where the EU**'s fabless ecosystem is underdeveloped**, there is limited market incentive for foundries to deploy manufacturing capacity in the EU. This is particularly the case for leading-edge semiconductors that are vital for AI chips utilised in AI gigafactories and factories, but also other lead markets and applications as explained above. Without a dense cluster of design firms generating consistent, high-value tape-outs, the business case for locating cutting-edge fabs in the Union remains weak. Foundries follow the gravity of demand: where design pipelines are active, risky and expensive nodes become commercially viable. Where those pipelines are sparse or fragmented, even generous public incentives struggle to outweigh the lack of a sustained customer base.

In 2023, according to estimates by International Data Corporation (IDC), the EU had 8.1% of global front-end manufacturing capacity, a share projected to remain constant until 2030 ([94]). When analysing this front-end footprint, one can see that here the EU has limited leading-edge capacity - which is all attributable to the Intel fab in Leixlip (Ireland), and sub-optimal levels of capacity for mainstream and legacy nodes. In back-end manufacturing, the EU largely relies on facilities in South-East Asia and European industry only keeps a small manufacturing footprint in the EU.

The current industrial structure is shaped by the needs of the EU's main industrial sectors, in particular automotive and industrial automation. Here, production is largely focused on more mature technologies such as sensors, microcontrollers and analogue circuitry, which while crucial, are largely lower-margin and are generally more sensitive to the cyclicality of the industry. When it comes to higher value-added segments of semiconductor manufacturing and design, the Union has a limited role. A direct consequence of being absent from leading-edge manufacturing is that the EU has also lost much of the skilled human capital needed to develop these capabilities domestically. **This imbalance leaves the EU vulnerable to geopolitical tensions and economic coercion** (see section 1.5.1. concerning the first problem driver) **over the manufacturing of advanced semiconductor technologies that underpin AI, telecommunications, security and defence.**

Cost structures further constrain the EU's competitiveness in manufacturing. As seen in **Figure 11**, fabrication costs in the US or Japan are approximately 16% lower than in the European Union. The gap with China, Taiwan and South Korea is even larger, with the cost of constructing a fab in South Korea estimated at approximately **half the cost of an equivalent facility** in the EU.

Semiconductor manufacturing in the EU faces a structural cost disadvantage driven by four main factors: capital, labour, land and energy. **Capital costs** represent the largest share of total fab production costs and are higher in the EU than in most competing regions, due to higher cost of equity, elevated country risk premiums, and the smaller scale and lower

([94]) This stable share must be viewed against a global backdrop in which manufacturing capacity is expanding rapidly. In absolute terms the manufacturing capacity of the Union has increased by over 38%, from 1.07 million wafers per month in 2023 to around 1.48 million wafers per month by 2030 if all investments materialise.

liquidity of European semiconductor firms. **Labour costs** are also structurally higher when measured in unit terms, as relatively high employer social security contributions and lower labour productivity offset the EU's slightly lower nominal wages. **Land costs** account for a smaller share of total costs and place the EU in an intermediate position internationally, being cheaper than in some Asian economies but more expensive than in the US and China.

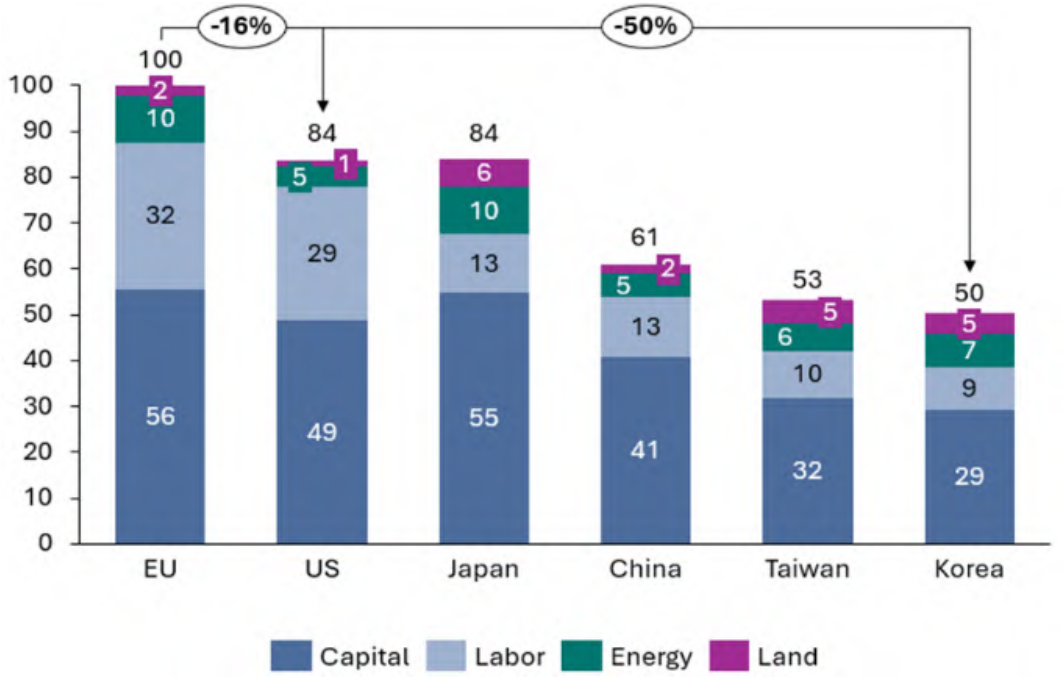

Figure 11 - Overall fabs production cost gap across countries (normalized EU = 100) Source: Yole/Decision[95]

When it comes to energy, prices are also significantly higher in the EU, with electricity costs being roughly double those in the US and China in recent years. ([96]) Beyond the initial capital expenditure, this drives up the costs of running fabs in the EU significantly. In addition, other regions benefit from denser supplier ecosystems, shorter supply chains and larger pools of specialised talent, all of which lower production and logistics costs.

Taken together, these factors result in a structural weakness in the EU's manufacturing capabilities. **This reality leaves the EU with limited capacity to compete in fast-growing segments and increasingly exposed to critical dependencies across technologies, from mature to leading-edge.** Furthermore, emerging fabless start-ups in the EU, active in segments such as AI chips, have to rely on fabrication in third countries. This dependence not only exposes them to geopolitical and export-control risks, but also lengthens development cycles, increases costs and reduces their ability to iterate rapidly. It also deprives the EU of the feedback loops between design and manufacturing that typically drive innovation clusters, making it harder for local start-ups to scale or anchor subsequent production in the Union. A

([95]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.
([96]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.

successful approach to change this situation, in the words of one participant of the evaluation, "must not only help develop production capabilities but, more fundamentally, it must create the framework conditions for industry to create […] an end-market for more semiconductors 'made in the EU'." ([97])

The Union's competitiveness challenge, combined with geopolitical pressures, underscores the urgency of **Union level action to accelerate permitting processes for Pillar II facilities, i.e. eventual integrated production facilities (IPF)/open EU foundries (OEF), while maintaining high environmental standards**. Approval procedures in the EU are significantly slower than in competing regions: industry reports indicate **permitting approvals take 10-18 months in the EU, compared with about 6 months in South Korea and Taiwan** and less than one month in certain other jurisdictions.

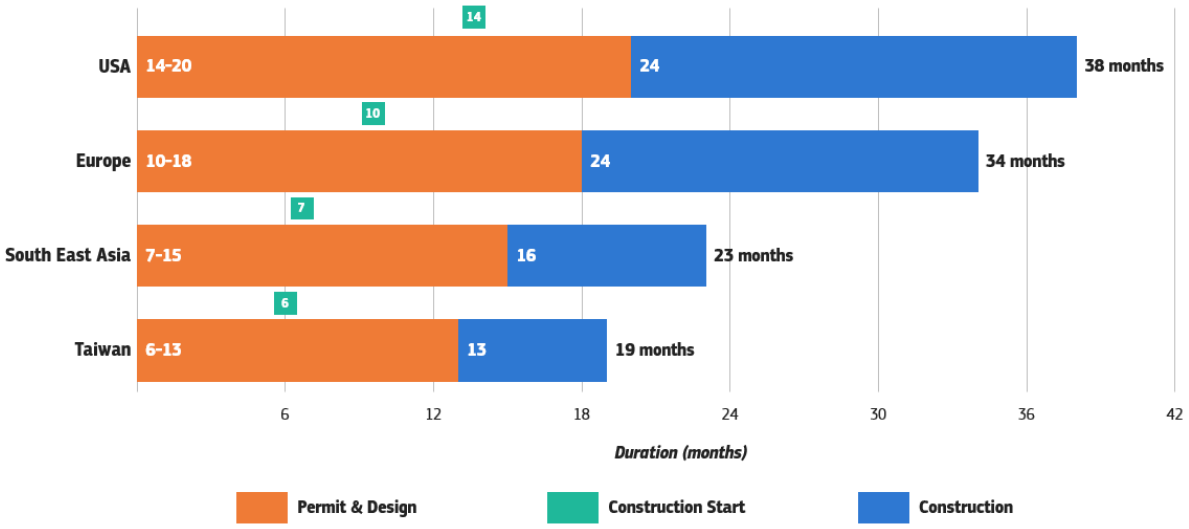

Figure 12 - Average duration of projects for building wafer fabs

Results from the evaluation align with these shortcomings. Respondents in the open public consultation highlighted insufficient manufacturing capacity, limited investment instruments, shortages of skilled labour, and weak domestic demand from hyperscalers and AI companies as the principal obstacles in the development of an EU AI-chip value chain. ([98]) A lack of venture capital and risk finance was reported as a particular constraint for design firms, while IDMs and other production-oriented firms pointed to lengthy permitting procedures and high energy costs as major impediments ([99]).

2.3.3 PD3: Insufficient support and advanced facilities for scaling up innovative start-ups

The EU's semiconductor sector suffers from a 'lab-to-fab gap', which describes the struggles to translate scientific excellence into products that are successful on the market. Despite

([97]) Annex 2 Section 5.
([98]) Annex 2 Section 4
([99]) Annex 2 Section 5.2.

remaining very competitive in terms of semiconductor R&D and scientific publications (**Figure 13**), European semiconductor manufacturers have steadily lost market share (**Figure 14**).

This loss in market share can be largely explained by the lack of market dynamism in the European semiconductor industry, with long time incumbents still dominating the market. In fact, all major players in European semiconductor manufacturing have their roots in companies founded over 70 years ago. ([100]) In device manufacturing, the product lines of European players are based on largely mature technologies. This is an anomaly given the substantial volume of cutting-edge semiconductor research produced within the Union, which should provide a strong foundation for the emergence of new European technologies on the market.

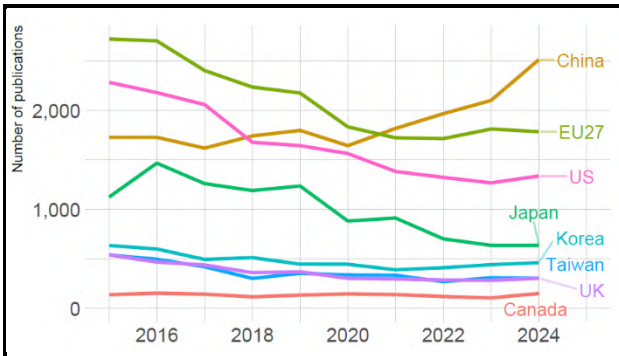

Figure 13 - Scientific publications related to semiconductors (Source: Open Alex article publications)

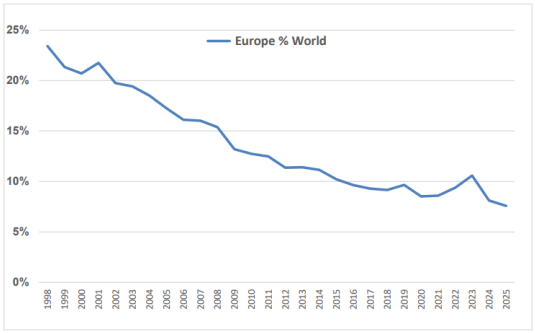

Figure 14 - European market share in the semiconductor industry (Source: Future Horizons May 2025)

This lack of dynamism is related to insufficient support for innovative start-ups in scaling up, a point that was also highlighted by the **Draghi and Letta reports**. ([101]) The results of the evaluation support this observation: participants in several workshops identified mobilising private capital, particularly European venture capital, as a structural bottleneck for the support of semiconductor design firms. ([102])

According to a recent European Investment Bank report ([103]), European deep-tech startups raised only 20% of the capital raised by their US peers in 2023. Here, the EU performs better in seed and early-stage funding, reaching over 50%of US levels, but this falls to around 10% for scale-up rounds, which are the stages at which semiconductor firms can focus on industrial deployment.

([100]) Referring to the 4 European IDMs i.e. STMicroelectronics, Infineon Technologies, NXP, Robert Bosch.
([101]) Enrico Letta (2024), Much more than a market
Mario Draghi. (2024). The future of European competitiveness: In-depth analysis and recommendations (Part B).
([102]) Annex 2 Section 5.3.
([103]) European Investment Bank publications: "The scale-up gap: Financial market constraints holding back innovative firms in the European Union" (July 2024).

Furthermore, only about 5% of global venture capital is raised in the EU, compared to 52% in US and 40% in China, meaning that much of the equity of European deep-tech companies is owned by non-European investors. Venture financing experts widely interpret this as a direct consequence of the persistent fragmentation of the European financial markets and the absence of a real Capital Markets Union, which limits the liquidity available for equity financing. This combined with a more risk-averse culture in the EU, limited insight into the semiconductor industry among investors, as well as fragmented markets and complex regulations make scaling-up across borders more difficult. Facing such challenges, start-ups are enticed to accept financing from the US or Asia, move their HQ to third countries, or are acquired by non-European firms to ensure industrialisation of their IP and financial returns, leading to the loss of strategic technologies, talent and future value creation for the EU.

Besides risk capital, the lab-to-fab gap could also be closed by more interaction between SMEs and academia. Workshop participants as well as interview partners report that SME access to the pilot lines established under Pillar I turned out to be difficult and prohibitively expensive. ([104])

Another relevant driver is the lack of leading-edge manufacturing and advanced packaging facilities in the EU, which are essential to bridge the so-called 'lab-to-fab' gap. Around semiconductor manufacturing hubs, dense ecosystems tend to emerge, attracting suppliers of equipment, materials, chemicals, as well as design houses, fabless as well as system companies from key user industries. This is because physical proximity shortens feedback loops, accelerates 'learning by doing' and enables tight collaborations on design-technology co-optimisation, rapid prototyping and qualification, which are crucial advantages for industrialisation, especially for smaller companies, as they reduce coordination costs and shorten development cycles. A clear example of such dynamic is the Hsinchu Science Park developed in Taiwan around TSMC, brimming with design houses, system companies and technology organisations, thus creating short idea-to-product cycles. However, linkages to industry are also required in the other direction, to the industrial users of advanced chips which are often not located in Europe. This leaves chip design firms without anchor customers a strong home market according to the public consultation. ([105])

In this context one can also observe that, since the 1980s, European policy initiatives (such as ESPRIT, JESSI, MEDEA, CATRENE, ECSEL, KDT and now Chips JU) have predominantly focused on research and development programmes, which has led to core R&D strengths and multiple research centres of excellence across the EU. However, as regards financial support to commercial undertakings and to industrial manufacturing facilities, the European regulatory framework, designed to support an effectively functioning Single Market while limiting distortions within the internal market, has in practice allowed public intervention on R&D but much less in support for its market exploitation and industrial deployment. This has over time left the EU at a competitive disadvantage vis-à-vis prevailing practices to offset massive capital expenditures in other regions, and has, in effect, contributed to the underdevelopment of high-tech industrial deployment in Europe.

([104]) Annex 2
([105]) Annex 2

Taken together, the above highlights the Union's limitations in financing advanced industrial facilities, via targeted public support schemes, to enable innovative semiconductor ventures to scale up in the EU and to contribute to its industrial competitiveness.

2.3.4 PD4: Lack of demand for European advanced chips from user industries

The EU is a significant market for semiconductors. According to recent estimates from IBS, the EU accounts for around **13% of global direct semiconductor demand**. ([106]) This figure refers to **components** shipped to European system companies, which in turn integrate them into intermediate goods or finished products. However, it does not capture the larger volume of chips already **embedded in imported finished products** that reach European customers, such as smartphones, laptops, servers, networking equipment or cloud infrastructure. This share is estimated to be at around **20% of global semiconductor demand**.

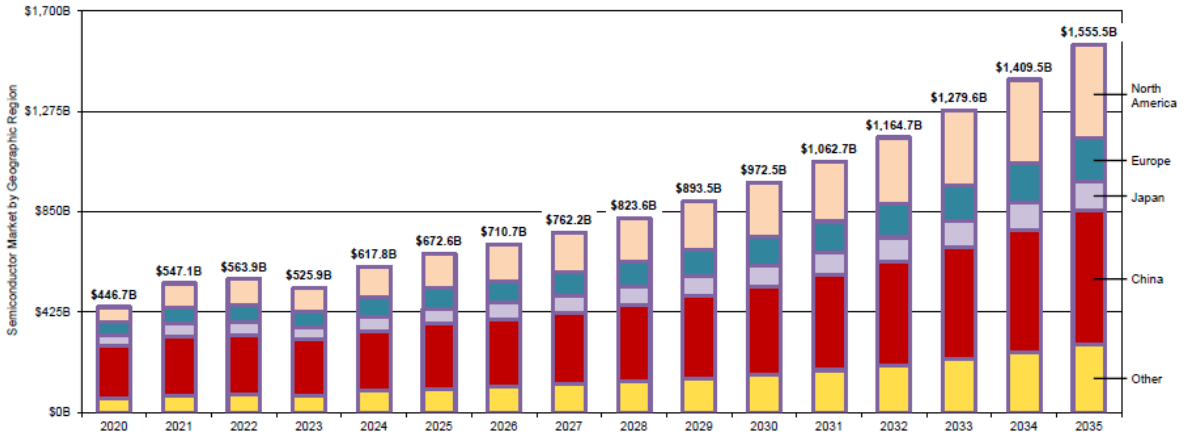

Figure 15 - Forecast of semiconductor demand by region. (Source: IBS, August 2025)[107]

Furthermore, the EU has a particularly distinctive direct demand profile, where semiconductor purchases by firms operating in the Union are oriented towards the **automotive** and **industrial** sectors.([108]) In 2023, the Union accounted for 39.4% of global demand for automotive semiconductors and 23.1% for industrial semiconductors.([109])This reflects the EU's strengths in power devices, microcontrollers, sensors and analogue components, which underpin many of the Union's industrial and automotive technologies. By contrast, the Union hosts relatively few OEMs or Tier 1 suppliers for consumer electronics, personal computing devices or hyperscale cloud infrastructure. Hence, while direct internal demand is skewed towards mature-node chips, much of its consumption of **leading-edge** semiconductors comes embedded in **imported systems**, making it hard for the EU to drive the industrial demand needed to develop an advanced fabless-foundry ecosystem purely on market grounds.

([106]) Demand from firms such as OEMs and Tier 1s that purchase chips as intermediate inputs.
([107]) IBS, Global Semiconductor Industry Service, Semiconductor Market by Application Part 1, February 2025.
([108]) EU's strengths and weaknesses in the global semiconductor sector, Publications Office of the European Union, Luxembourg,2025, https://data.europa.eu/doi/10.2760/6302476, JRC141323.
([109]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.

The biggest change in EU demand patterns in recent years was the rapid demand growth for AI chips. The **datacentre/AI/cloud** segment of the semiconductor market already represents over 18% of European semiconductor consumption and is expected to reach around **26% by 2030.** ([110])

However, an estimated 96% of the semiconductor market for datacentres is captured by US-owned companies ([111]) which contributes to a significant trade deficit between the EU and the US and creates critical dependencies on third-country suppliers in what is currently the fastest growing economic sector. Moreover, the US administration, despite rescinding the Framework for Artificial Intelligence Diffusion, is now advancing on an AI Action Plan built around exporting a "full stack" solution of chips, models, software and standards with strict conditionality. This implies a **significant strategic risk for the EU's sovereignty, as its AI infrastructure and software** will potentially be structurally dependent on extraterritorial US jurisdiction and policy choices.

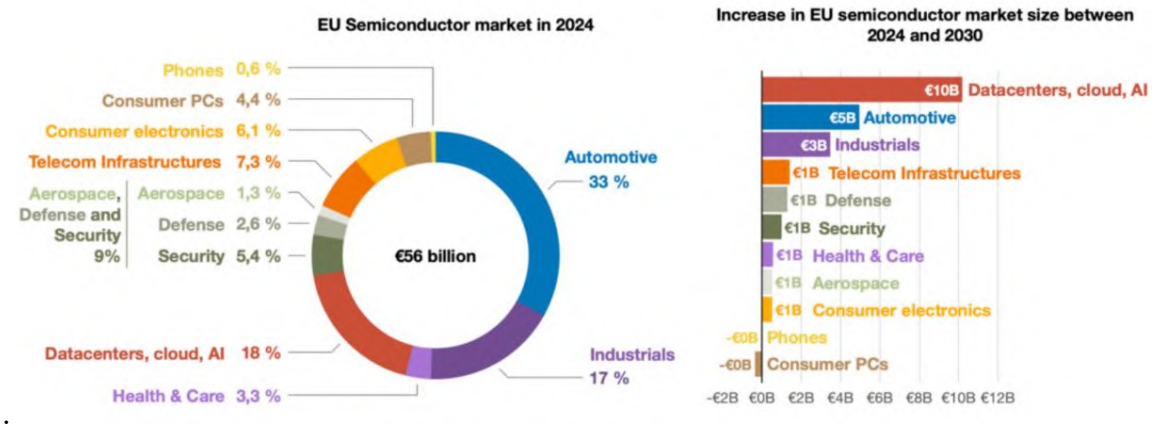

Figure 16 - Semiconductor consumption and absolute increase in market size by application area (Source: Decision based on Eurostat and WSTS)

Competitive pressure in **mature** and **mainstream** technology nodes has intensified as third countries expand subsidised production capacity. For example, China has substantially increased investment in mature-node manufacturing as part of its self-sufficiency strategy and complemented it with 'China for China' policies that prioritise domestic sourcing. ([112]) These developments have added pressure in segments where many European companies operate. Global semiconductor demand, however, is growing most rapidly in segments where the EU currently has limited direct presence.

Strong investment in data centres, AI systems and cloud services is driving demand for high-performance computing, memory and advanced logic chips, which are segments of the industry in which the EU is weak. ([113]) In fact, no EU headquartered company has any

([110]) Decision Etudes & Conseil and YOLE Group, Competitiveness of the EU semiconductor manufacturing industry, Nov.2025.
([111]) Cloud and AI Development Act Impact Assessment.
([112]) China asks carmakers to use up to 25% local chips by 2025
([113]) Europe is losing out big time on the AI and data centre battle | articles | ING Think

leading-edge manufacturing capacity for both logic and memory. Furthermore, as seen in **Table 2**, when looking at the historical and projected number of design starts in the EU at ≤7nm (an indicator of design activities for leading-edge semiconductors), the EU has been and is expected to continue to be a minor player.

Metric	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Design starts (≤7nm)	4	9	14	19	26	38	60	91	123	157	194
Percent Europe (%)	0.65	1.30	0.97	1.29	1.72	1.22	1.87	2.17	2.83	3.48	4.14

Table 2 - Design starts in Europe ≤7nm (Source IBS Monthly Report June 2024)

TSMC reported that orders linked to high-performance computing accounted for roughly 60% of its revenue in Q2 2025, reflecting growth in AI chips, networking base stations, PCs and game consoles. ([114]) Analysis by McKinsey expects these trends to persist, with AI processors forecast to grow with a CAGR of 18-29% annually between 2023 and 2030, and memory chips at a CAGR of around 17-23%, with AI and computing chips capturing over 50% of global semiconductor market growth until 2030. As the whole semiconductor market will grow at a rate of 8-9% annually until 2030, the other semiconductor sectors are expected to expand at a slower pace, hence the EU's share of the global market is expected to diminish further.

Markets for mature-node chips are also under pressure due to changes in demand profile. For example, in **automotive**, the industry is shifting towards more centralised, software-defined architectures with very powerful real-time central processing units **required for the increasingly autonomous and connected vehicles**. As of today, such processors are supplied by non-EU vendors, such as Nvidia, Qualcomm and Intel (Mobileye), often reusing elements of architectures originally developed for smartphone, datacentre or edge-AI inference workloads adapted for automotive-grade requirements. By 2030, around 30-35 million vehicles per year running on ADAS[115] Level 2+ to Level 4 systems, including 6-8 million from European carmakers, are likely to require such central high-performance processors ([116]).

In **telecom** networks, baseband units and edge nodes require high-speed processors in 5G and forthcoming 6G deployments: by 2030 European equipment vendors may require up to 1 million units per year. Furthermore, emerging applications in industrial **automation, robotics, defence and security** will require energy efficient, high-performance AI processing chips at the edge, and the combined EU-linked demand may be estimated at up to 1 million units per year in the period 2030-35 ([117]). Finally, a promising new consumer market segment

([114]) 2Q25 Presentation (E) Note: for TSMC, HPC includes PCs, tablets, game consoles, servers, base stations and more (see 2024 Business Overview_0.pdf)
([115]) Advanced Driver Assistance Systems
([116])https://www.mckinsey.com/industries/automotive-and-assembly/our-insights/mapping-the-automotive-software-and-electronics-landscape-through-2030
([117]) Estimates based upon market forecasts from ABI Research, Goldman Sachs, Markets and Markets, Fortune Business Insights and other analysts on edge AI markets and robotics.

is the one of **smart glasses ([118])**, that could generate demand in the order of millions of high-end embedded processors per year, and where the EU is potentially well positioned.

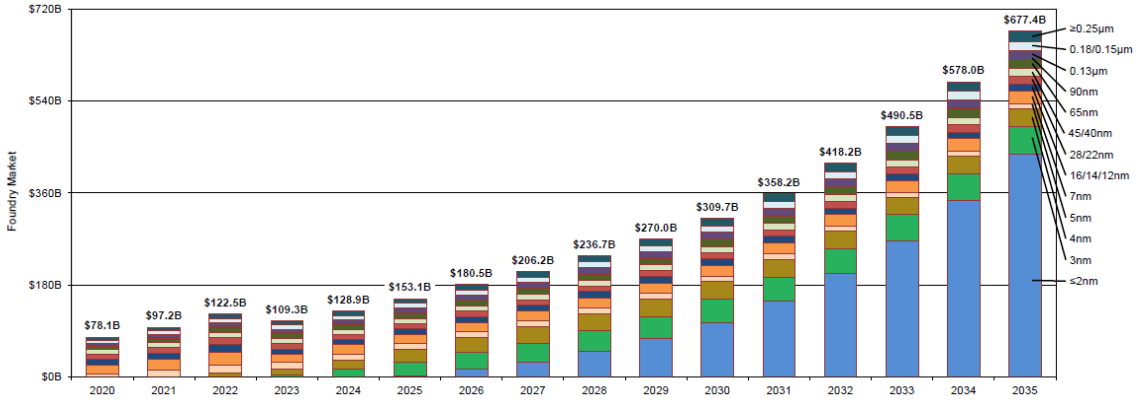

Figure 17 - Foundry market by technology node (source IBS, February 2025)

The EU semiconductor industry could make use of its established experience with automotive and industrial customers to capture higher added-value markets or move into these next generation technologies. However, challenges in this regard include: the lack of demand aggregation, as these sectors rely on customisation or relatively low volumes compared to AI data centres and smartphones; and the steep up-front investment required for developing more leading-edge technologies. Workshop participants described this as a fundamental structural weakness since fragmented demand has prevented economies of scale, limiting Europe's ability to industrialise emerging technologies ([119]).

It is therefore clear that unless the EU succeeds in channelling demand from these downstream markets towards European solutions, entire swaths of the EU's industrial base could be locked into third country technologies, thus limiting opportunities for the development of European alternatives and exposing the Union to potential economic coercion.

2.3.5 PD5: Insufficient information available to public authorities on the resilience of the European semiconductor supply chain

The Evaluation of the Chips Act clearly showed that while coordination between the Commission and Member States has significantly improved via the European Semiconductor Board (including information on possible disruptions, such as in the *Nexperia case*), the crisis preparedness framework still remains insufficient, for the following reasons:

- The Pillar III framework is largely reactive in nature, with the toolbox of measures being applicable only after a crisis stage is activated. Preventive actions are carried out only after alerts are received in line with Article 22 of the Chips Act.

([118]) Smart glasses are wearable devices integrated into eyeglass frames that combine miniaturised displays, cameras, sensors, and wireless connectivity to deliver augmented reality experiences and hands-free computing. Applications span industrial maintenance, healthcare, logistics, defence, and consumer use.
([119]) Annex 2 Section 8

- The preventive actions the Commission and Member States can undertake before the activation of the crisis stage remain limited in nature ([120]).
- The boundaries of when public intervention (preventive action) is warranted before a crisis stage is activated are not set.
- There is limited EU visibility into semiconductor supply chains, coupled with the complexity of said supply chains, makes it almost impossible to assess when to intervene. The types of information that are missing are different in nature (depending on the technology used, type of semiconductor product or process etc.) but often revolve around supply chain data such as supplier relationships, capacities, inventory levels etc. Such information is at the hands of the industry.

In the current context, the semiconductor supply chain remains highly vulnerable to disruptions due to its structural complexity, fragmentation, and reliance on a limited number of actors at critical stages of the supply chain. Recent trade restrictions, including those arising from the COVID-19 pandemic, restrictions imposed on AI chips ([121]) and critical raw materials ([122]), as well as concerns about overcapacity in mainstream semiconductor segments ([123]), have demonstrated that the Union currently lacks sufficient crisis preparedness capabilities required for timely, decisive and effective action.

Operational capacities for supply chain monitoring, risk assessment, and crisis management at both Union and Member State levels also remain limited. Although the European Semiconductor Board and initiatives under Pillar III of the Chips Act have established an architecture for supply chain monitoring with mandatory data collection in times of crisis (Article 25), and encouragement of voluntary data sharing (Articles 19 and 20), it does not establish broader compulsory data-sharing mechanisms comparable to those existing, for example, in the US where data disclosure can be mandated for national security purposes ([124]). As a result, public authorities are constrained in their ability to anticipate risks, model disruption scenarios, or assess emerging market developments.

The resources and tools available, particularly in terms of specialised staff and analytical expertise, are also insufficient to ensure continuous and real-time situational awareness. Current tools do not yet support advanced forecasting, rapid information-sharing, or coordinated response planning.

([120]) Under Article 22 of the Chips Act, the Commission shall convene an extraordinary meeting of the European Semiconductor Board, composed of Member States representatives, to discuss the severity of the supply disruptions, whether to activate the crisis stage, whether to carry out joint procurements, and to discuss with stakeholders to identify and prepare potential preventive measures. The Commission shall also enter in consultations with relevant third countries to seek cooperative solutions.

([121])https://ec.europa.eu/commission/presscorner/api/files/document/print/en/statement_25_255/STATEMENT_25_255_EN.pdf

([122]) https://www.technologyreview.com/2023/07/10/1076025/china-export-control-semiconductor-material/

([123])https://ec.europa.eu/commission/presscorner/api/files/document/print/en/statement_24_1828/STATEMENT_24_1828_EN.pdf

([124]) Under the US Trade Act of 1974, Section 301 is designed to address “unfair foreign practices affecting U.S. commerce”. Section 301(b) can also be used to respond to “unreasonable or discriminatory foreign government practices that burden or restrict U.S. commerce”. Under Section 302(b), the U.S. Trade Representative may self-initiate an investigation under Section 301.

Structural features of the global semiconductor market further compound these preparedness gaps. The sector's strong cyclicality, high capital and knowledge intensity, long production lead times, and significant geographic concentration create systemic vulnerabilities that can amplify even minor disturbances. Without robust monitoring and crisis-response capacities outside of the formal crisis stage under the Chips Act, such vulnerabilities can quickly translate into supply chain disruptions with significant economic and societal consequences.

However, on data gathering under Pillar III, industry stakeholders have expressed legitimate concerns about sharing sensitive information, including commercially confidential data and trade secrets. Strengthened coordination mechanisms, clearer safeguards including EU antitrust compliance, and trust-building measures are required to mitigate these concerns, but they are not yet sufficiently developed.

Taken together, these factors mean that the EU lacks the necessary preparedness to identify, anticipate, and mitigate semiconductor supply chain crises in a timely and coordinated manner.

2.4 How likely is the problem to persist?

There is limited evidence to suggest that the challenges outlined above are transient. Three structural factors indicate that the current problems are likely to persist over medium to long-term.

First, **geopolitical tensions are expected to endure if not further intensify**. These tensions are not driven by short-term political cycles but by long-term shifts in the global balance of power that are leading to persistent competition in the domains of security, technological supremacy ambitions, economic influence, and global governance. The sector's centrality to advanced AI systems and defence capabilities has further elevated its geopolitical significance, resulting in the adoption of far-reaching industrial policies and increasing export controls. Recent measures to restrict the access to AI chips (US) and critical raw materials (China) demonstrate a continued willingness by the US and China to leverage economic dependencies for strategic purposes.

Second, **the semiconductor value chain remains structurally fragile and highly exposed to disruption**. Multiple bottlenecks and a high concentration at different stages of the value chain, from advanced manufacturing of logic chips to materials and equipment, make interruptions likely. While significant investment is underway in the EU, including projects supported under Pillar II of the Chips Act, there are still gaps in capacity ([125]). At the same time, the high degree of geographic concentration in several critical segments of the value chain increases the system's vulnerability to natural disasters and other supply shocks. Even minor disturbances can propagate rapidly across the chain and impact well beyond the initial point of failure. Until additional European capacity becomes fully deployed, the ecosystem will remain inherently prone to instability.

([125]) Special report 12/2025 - The EU's strategy for microchips

Finally, **the ongoing expansion of semiconductor production capacity in Asia and the US, supported by substantial public support,** is currently outpacing the EU. All leading semiconductor players (China, Japan, the US, South Korea, Taiwan) are intensifying their industrial strategies, expanding fabrication capabilities and consolidating domestic supply chain ecosystems. This sustained momentum indicates that competitive pressure on European manufacturers will not diminish: rather, it is expected to increase as other regions continue to scale leading-edge manufacturing capacity, thus cementing long-term strategic advantages.

3 WHY SHOULD THE EU ACT?

3.1 Legal basis

The current legal bases of the Chips Act Regulation are Article 173(3) and Article 114 of the Treaty on the Functioning of the European Union (TFEU). The Union shall contribute to the achievement of the objectives set out in Article 173(1) TFEU through the policies and activities it pursues, as these objectives are to ensure that the conditions necessary for the competitiveness of the Union's industry exist. In accordance with a system of open and competitive markets, actions are aimed at: speeding up adjustment of industry to structural changes; encouraging an environment favourable to initiative and to the development of undertakings throughout the Union, particularly small and medium-sized undertakings; encouraging an environment favourable to cooperation between undertakings; fostering better exploitation of the industrial potential of policies of innovation, research and technological development. The objective of Article 114 TFEU is the establishment and functioning of the internal market by enhancing measures for the approximation of national rules.

A new legislative act would have the same legal bases as the current Chips Act Regulation. New actions would ensure the conditions necessary for the competitiveness of the Union's industry and improve the level playing field for companies in the internal market, subjecting them to the same requirements across the Union.

Regarding the legal basis of Article 173(3) TFEU, Article 6 TFEU notes that the Union shall have competence to carry out actions to support, coordinate or supplement the actions of the Member States. These areas of action include industry, according to Article 6(b). With regard to the legal basis of Article 114 TFEU, Article 4(1) TFEU notes that the Union shall share competence with the Member States where the Treaties confer on it a competence which does not relate to the areas referred to in Articles 3 and 6. Article 4(2)(b) further notes that shared competence between the Union and the Member States applies in area of the internal market.

As the initiative is subject to shared competence according to Article 4 TFEU and the competence to support, coordinate or supplement according to Article 6 TFEU, compliance with the subsidiarity principle must be ensured. In the case of Article 173(3) TFEU, actions taken should not entail the harmonisation of national laws and regulations but reinforce the competitiveness and resilience of the semiconductor industrial base. The current Chips Act and any new legislative act building on the Chips Act Regulation bolster the strength and resilience of the European semiconductor technology and industrial landscape, enhancing the innovation potential of the semiconductor ecosystem throughout the EU. This includes lowering the reliance on a small set of non-EU companies and regions and expanding the EU's ability to design and manufacture advanced semiconductors. The Chips for Europe Initiative (Pillar I), which will continue to be supported through the new legislative action, is

intended to help achieve these goals by closing the gap between the EU's research excellence and its effective, sustainable industrial deployment.

3.2 Subsidiarity: Necessity of EU action

The objectives of the proposed actions cannot be achieved sufficiently by Member States acting alone. The economic activities relating to the semiconductor industry across the Single Market are deeply integrated. Semiconductor industry resilience across the Union cannot be effective if approached in a severed manner through national or regional silos. The Chips Act came to address this shortcoming, by setting a common Union framework. The challenges of over-dependence on third country semiconductor supply chains and limited crisis-preparedness capacities manifest differently at national, regional and local levels, due to the variation in national industrial sectors and levels of technological capability. Across the EU, however, the problem is broadly widespread rather than confined to a few countries, because all Member States, regardless of their own manufacturing footprint, are deeply embedded in integrated European value chains that rely on globally concentrated design and manufacturing of semiconductors. The underlying causes of these vulnerabilities are the same across the EU, stemming from the globalisation of the semiconductor industry. While Member States can deploy certain measures individually, such as investment incentives, national semiconductor strategies and workforce programmes, they generally lack the scale, coordination mechanisms, and market-steering power needed to address structural dependencies in a globally concentrated industry. Relying solely on national action risks fragmentation, distorting the single market in ways that run counter to Treaty principles or undermine the interests of other Member States competing for the same investment or supply contracts. The problem is inherently cross-border, given the pan-European nature of semiconductor value chains, the interconnectedness of R&D ecosystems, and the fact that disruptions in one Member State can rapidly propagate through the internal market. Leaving action to Member States alone would increase costs and inefficiencies, as parallel and uncoordinated national initiatives would duplicate efforts, dilute bargaining power, reduce interoperability of preparedness measures, and ultimately fail to achieve the scale required to meaningfully reduce the EU's strategic dependencies.

3.3 Subsidiarity: Added value of EU action

The objectives of strengthening the EU's semiconductor design and manufacturing capacity and improving crisis-preparedness can be achieved more effectively at Union level, since the scale and systemic nature of the challenges exceed the capacity of individual Member States acting alone. Significant economies of scale arise when coordinating investment in large-scale manufacturing facilities, shared R&D infrastructure, and cross-border early-warning and monitoring systems, meaning that EU-level action can pool resources, reduce duplication, and deliver outcomes more efficiently than fragmented national efforts. Measures such as the ramping up of production capacities, the speeding up of permitting, priority rated orders and common purchasing aim to ensure a coherent response to future crises and to avoid the fragmentation of the Single Market.

A common policy framework also brings clear benefits, as it replaces divergent national incentives, crisis-response protocols, and reporting standards with common approaches that ensure coherence, reduce administrative burdens, and avoid subsidy races or inconsistent regulatory requirements. The functioning of the internal market is thereby improved, since

coordinated EU action minimises distortions, ensures fair competition for attracting semiconductor projects, facilitates the smooth circulation of critical inputs and chips, and strengthens the resilience of cross-border supply chains that depend on seamless integration across Member States.

4 OBJECTIVES: WHAT IS TO BE ACHIEVED?

4.1 General objectives

The original Chips Act had two general objectives: ([126])

1. To ensure the conditions necessary for the competitiveness and innovation capacity of the Union, to ensure the adjustment of the industry to structural changes. This involves strengthening the EU's research, development and innovation leadership to help the semiconductor industry adjust to structural changes. This is primarily addressed by Pillar I, the "Chips for Europe Initiative", which focuses on bridging the 'lab to fab' gap.
2. To improve the functioning of the internal market by laying down a uniform Union legal framework for increasing the Union's long-term resilience and its ability to innovate and provide security of supply in the field of semiconductor technologies. This objective focuses on increasing the Union's resilience and security of supply in the field of semiconductor technologies. This is primarily addressed by Pillar II, which creates a framework to support "first-of-a-kind" manufacturing facilities, and Pillar III, which establishes a coordination mechanism for monitoring, crisis prevention and response.

The proposed Chips Act 2.0 builds on these objectives with two new general objectives:

1. Increase the competitiveness of the European semiconductor value chain to improve its technological sovereignty and resilience, by accelerating the industrial deployment of research and innovation, ensuring security of supply and reducing strategic dependencies in cutting-edge and mature semiconductor technologies.
2. Enhance crisis preparedness to ensure the EU's security of supply, by increasing the resilience of the European semiconductor supply chain and protecting EU's economic security.

The original Chips Act and the proposed Chips Act 2.0 share a common overarching aim, i.e., **strengthening the Union's semiconductor ecosystem**, but they differ in emphasis and conceptual framing. The evolution is characterised by a shift from a predominantly innovation and internal-market-driven logic towards a **more explicit strategic resilience and technological sovereignty framing**, with stronger focus on supply-chain dependencies and crisis preparedness. Chips Act 2.0 widens the competitiveness and innovation rationale to a broader value-chain perspective and explicitly links competitiveness to the Union's technological sovereignty and resilience. Compared to the original formulation, the Chips Act 2.0 objectives place greater emphasis on accelerating the lab-to-fab transition. This implies an emphasis on ensuring that research and innovation activities translate into not only excellence and leadership but also greater security of supply, and a reduction of strategic dependencies across both cutting-edge and mature semiconductor technologies.

([126]) Article 1 Chips Act, Regulation - 2023/1781 - EN - EUR-Lex

Furthermore, Chips Act 2.0 elevates crisis preparedness as an explicit general objective, connecting it directly to the Union's security of supply and economic security. While the original Chips Act contains crisis monitoring and response mechanisms under Pillar III, these are conceptually embedded within the objective of improving internal market functioning and ensuring resilience through coordination. The revised framing treats crisis preparedness as a systemic imperative, including outside of declared crises.

While mirroring the general objectives of the original Chips Act, these new general objectives represent a targeted evolution of the current regulation, specifically designed to address the identified problems and their drivers identified in Chapter 2. The new objectives reflect the growing economic security risks created by rising geopolitical tensions and incorporate this dimension into the earlier policy framework.

4.2 Specific objectives

As set out in the intervention logic, the proposed Chips Act 2.0 pursues the following specific objectives:

- SO1: Enhance the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips
- SO2: Develop a strong user market across key industry sectors
- SO3: Increase intelligence capabilities for crisis preparedness and response

5 WHAT ARE THE AVAILABLE POLICY OPTIONS?

5.1 What is the baseline from which options are assessed?

5.1.1 Current state-of-play

The annexed Evaluation report finds that the Chips Act successfully created a European semiconductor regulatory and policy framework within a notably short timeframe, where none previously existed. Through the three pillars of the Chips Act, it mobilised significant public and private investment, established state-of-the-art EU-level infrastructures, and introduced governance mechanisms to support coordination and crisis preparedness. Stakeholder confidence in the overall strategic direction remains high ([127]), and the Act is widely regarded as a necessary response to geopolitical, technological, and economic pressures. The EU has strengthened its semiconductor research, innovation and early-stage manufacturing base, primarily through EU-level infrastructures such as pilot lines, competence centres and shared facilities, which have improved coordination and reduced duplication across Member States. Access to advanced tools and cross-border collaboration has increased, although several initiatives remain too recent to permit a meaningful assessment.

([127]) See Annex 2 Section 4 "Comparison of the results of consultation activities" for a nuanced assessment

Progress towards large-scale manufacturing deployment and strategic autonomy has taken place and the EU has increased its manufacturing capacity by 30%. ([128]) However, long lead times ([129]) mean new investments have not yet translated into production and a key investment project for a leading-edge chip manufacturing facility has been cancelled. ([130]) One must also consider that the structures of the semiconductor industry are characterised by strong path dependencies. Therefore, rebuilding a semiconductor ecosystem of specialised suppliers and service firms takes time, and success does not come immediately. As a result, the EU continues to depend structurally on non-EU suppliers in critical segments, particularly for advanced nodes.

Furthermore, the lab-to-fab gap persists ([131]). While the original Chips Act has raised technology readiness levels, the main challenge has shifted from innovation to industrialisation and scale, with pathways to volume manufacturing still difficult to realise. Scaling constraints are reinforced by limited private capital. Despite significant public funding, late-stage and institutional investment remains weak, reflecting structural features of the European financial system (capital market in particular) and limiting value capture in the EU.

Supply security instruments have improved coordination, but manufacturing deployment remains driven by national frameworks and firm-level decisions. Fragmented markets, weak demand aggregation and limited procurement coordination undermine the commercial viability of new capacity. Finally, EU-level visibility over semiconductor supply chains remains partial. Coordination and early-warning mechanisms have improved, but fragmented access to sensitive data limits system-level monitoring and crisis preparedness.

5.1.2 Economic impacts

5.1.2.1 Expected EU semiconductor firms' revenues

Semiconductor firms' revenues

The baseline or 'business as usual' (BAU) scenario shows that the revenues of EU's semiconductor firms, as set out in Annex 4, will expand at a 7.7% CAGR by 2030, and then reduce to 5% from 2030 to 2035. This drop is explained by the expectation that without more leading-edge capacity, the mature node profile of the European semiconductor industry will become less industrially relevant ([132]) in a market that will increasingly by dominated by AI, as discussed in Section 1.1 and in Annex 4.

Semiconductor value chain

([128]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.
([129]) See Annex 2 Synopsis of the stakeholder consultation activities, section 3.5.2.
([130]) See detailed analysis of the Intel's proposed semiconductor fab in Magdeburg, Germany, and its cancellation, in the Evaluation Report - section 4.1.1.2 on Pillar II.
([131]) See Annex 2, sections 3, 4 and 6.
([132]) IBS Global Semiconductor Industry Service – Analysis of Foundry Market – December 2025

Looking at **the broader value chain,** in a BAU scenario, the EU's strengths in **capital equipment** results in gaining market share from 27.9% in 2023 to 33.5% in 2030 in that segment. This growth is driven primarily by the expected continued dominance of ASML in photolithography, an important chokepoint in both the semiconductor and AI value chain, and the opportunities that arise for EUV lithography machines in the global ramp-up in manufacturing capacity driven by AI. Nevertheless, this dominance in photolithography is increasingly threatened ([133]), not least from weak demand in Europe, ([134]) and conceals key gaps in a multitude of other tools required for front-end and back-end manufacturing as well as packaging, assembly and testing, as discussed in section 8.1.3 of Annex 4.

Segment	**2023**	**2030**
IP	0.3%	0.4%
EDA	20.6%	17.9%
Capital equipment	27.9%	33.5%
Materials	16.8%	18.7%
Substrates	*20.5%*	*22.7%*
Other materials	*15.9%*	*17.4%*
Semiconductors	10.1%	9.6%
Fabless	*0.8%*	*2%*
IDM	*17.7%*	*16.6%*
Foundry	0.9%	0.5%
OSAT	0.0%	0.0%
Total value chain share	**11.7%**	**11.6%**

Table 3 - The EU semiconductor value chain share of revenues (Source: IDC)

As seen in **Table 3**, the EU's foothold in IP blocks, essential for reusing functions in design, will remain marginal, with its share of revenues rising only slightly from 0.3% in 2023 to 0.4% by 2030. This leaves the Union reliant on a small number of foreign suppliers for essential building blocks that underpin both advanced logic and specialised domain-specific designs. Similarly, when it comes to **Electronic Design Automation** tools, the EU will continue to rely on third-country providers for the essential design flows needed to produce state-of-the-art chips, while capturing 17.9% of global revenues by 2030, down from 27.9%

([133]) How China built its 'Manhattan Project' to rival the West in AI chips | Reuters
([134]) Annex 2, Section 4, 5 and 6.

in 2023. Any tightening of export controls or licensing requirements could directly constrain the Union's capacity to design and manufacture competitive semiconductors, including in high performance computing, AI, automotive and security-sensitive applications.

In **materials**, while the EU is expected to have a market share of 18.7% in 2030, up from 16.8% in 2023, 75% of specialty gases at the purity level required for semiconductors will still be sourced outside the EU, with over 50% of them relying on supply chains heavily dependent on China. ([135]) This adds on the dependencies on third countries for critical raw materials such as gallium, which are addressed under other legislative initiatives such as the Critical Raw Materials Act. ([136])

Between 2000 and 2022, the number of **Printed Circuit Board** (PCB) manufacturers in the EU, crucial for the broader electronics ecosystem, dropped from around 560 to less than 175, and the EU's share of revenues dropped from 16% to around 2.3%([137]). The sector remains highly fragmented and dominated by small firms, and the overall market-share trajectory continues to decline. As things stand, only a limited group of European suppliers are able to meet the technological demands created by rapid advances in semiconductors ([138]).

Under the business-as-usual scenario, fragmented and uncoordinated investment across Member States limits the Union's ability to develop competitive complementary capacity along the full semiconductor value chain, thereby increasing dependence on global suppliers and vulnerability to disruptions. Therefore, the Union will **retain critical vulnerabilities and weaknesses** across the value chain, which renders the EU unable to ensure a resilient and secure supply of semiconductor technologies.([139])

5.1.2.2 Manufacturing capacity

The BAU scenario conditions allow for the expansion of the EU's manufacturing footprint, resulting in tangible growth in domestic output and reversing earlier decline. By the end of the decade, the EU's semiconductor manufacturing capacity expands moderately in scale and technological capability: several new and expanded fabs come online, including the STMicroelectronics FD-SOI fab in Crolles (France), the GlobalFoundries foundry in Dresden (Germany), the Intel fab in Leixlip (Ireland), Infineon's Smart Power Fab in Dresden, the ESMC foundry in Dresden, the SiliconBox advanced packaging site in Novara (Italy), and several SiC/GaN wafer and device facilities.

Despite an increase in manufacturing capacity of 30% - from 1.07 million wafer starts per month to 1.39 million wafer starts per month, the EU**'s share of global semiconductor production remains at 8.1% by 2030** due to commensurate global expansion**.** This expansion in absolute terms will strengthen Europe's front-end and back-end manufacturing base and deepen established clusters. These investments also help Europe reinforce ecosystem resilience by sustaining activity in upstream segments, such as equipment and specialty

([135]) See stakeholder consultation in Annex 2.
([136]) Regulation - EU - 2024/1252 - EN - EUR-Lex
([137]) European Institute for PCB Community (EIPC).
([138]) IPC, Towards a Silicon to Systems Industrial Strategy, 2025.
([139]) Annex 2 Sections 4, 5 and 6.

materials, where European firms hold globally competitive positions without primarily depending on EU-based demand.

The expansion through 2030 should also be viewed in the context of unprecedented State aid provided by Member States, as well as COVID-19–related shortages that incentivised suppliers to expand manufacturing capacity. Beyond 2030, assuming all other factors remain constant, growth is expected to stabilise, shifting primarily to brownfield expansion with more moderate annual growth of 1-3%. As discussed in PD2, environmental and resource constraints, such as rising electricity consumption, water stress in key regions, and lengthy permitting processes further limit the pace at which the EU can expand or upgrade its manufacturing base. **However, under the business as usual scenario, leading edge node manufacturing remains very limited**. In 2023, the EU has limited ≤7 nm foundry capacity. ([140]) By 2030, the EU's leading-edge capacity by Intel in Ireland may ramp-up, but its foundry service volume will continue to remain modest in absolute terms. Even within the broader ≤28 nm category, capacity is limited, with the largest investment of the Chips Act, the ESMC foundry, becoming fully operational only in 2028. The EU's installed base in 2023 is largely at ≥40 nm, with mainstream and advanced nodes representing only a very small share of projected capacity by 2030. ([141])

As a result, the EU's front-end manufacturing profile will remain strongly **skewed toward >28 nm nodes** serving automotive and industrial demand. At the same time, EU semiconductor demand, particularly in automotive, industrial automation, and energy systems, continues to grow faster than domestic supply. In 2023, European semiconductor consumption amounted to roughly EUR 50 billion and is projected to expand at 5-6% annually under the BAU scenario, with automotive demand alone growing at about 8.2% CAGR between 2023 and 2026 ([142]).

Under the BAU scenario, ramping up manufacturing capacity in Europe would remain slower than other competing regions, as set out in PD3. Article 18 of the Chips Act already grants the semiconductor industry 'the most rapid treatment' possible under national legislation: however, it does not set thresholds for permitting times resulting in inconsistent application across Member States, and as such has not significantly reduced permitting times as discussed in PD3.

In terms of technological sovereignty, BAU developments strengthen but do not transform the EU's position. This increase in output will be largely concentrated in the EU's established strengths, such as wide-bandgap semiconductors and mature technologies. These technology families underpin core EU industrial sectors, and the additional capacity helps meet part of the demand from automotive, industrial automation and energy applications. However, **the Union does not establish a competitive foothold in leading-edge logic and memory segments**, where global innovation cycles are fastest, and margins are higher.

([140]) IDC, Semiconductors market data by feature size, sector and region, CNECT/2022/MVP/0084 – Second Interim Report.
([141]) Source Yole/Decision internal report. Market 2030 outlook.
([142]) See Annex 4.

These challenges are compounded by Europe's limited advanced packaging and system-integration capabilities, at a time when global competition is shifting toward heterogeneous architectures, chiplet integration, and 3D packaging.

5.1.2.3 Demand

On the demand side, over the coming years, a steep roll-out of **AI infrastructure** and data centres is expected, driven by the adoption of AI in society, AI Gigafactories and the future Cloud and AI Development Act. In fact, **EU data centre capacity demand is expected to quadruple from 2025 to 2030,** and to go from **12GW to 61.5 GW** in 2036 ([143]).

European consumption will continue to outpace domestic production, driven by **automotive**, **industrial automation**, **energy** applications and the ramp-up in **AI data centre** infrastructure. In fact, it is projected that EU demand will expand considerably faster than domestic supply, with an expected CAGR of 7.47% until 2035.([144]) Therefore, the gap between the EU's consumption and production widen through 2035, reinforcing high levels of import dependence despite rising capacity.

While the EU will invest heavily in AI Factories and Gigafactories in line with the AI Continent Action Plan, and improved conditions under the Cloud and AI Development Act are expected to spur additional private investment in data-centre capacity, the Union will still **remain reliant on third-country suppliers for AI chips** for both AI training and inference.

5.1.2.4 The cost (price) competitiveness of the EU industry

As analysed in Annex 4 Section 1.1, under a BAU scenario, the EU semiconductor manufacturing ecosystem is expected to remain less competitive than leading Asian manufacturing hubs. As set out in **PD2**, structural cost disadvantages persist across the value chain. EU-based fabs continue to face higher construction and operating costs, longer permitting and build-and-commission timelines, and weaker agglomeration effects than competitors in East Asia. This is also supported by interviews, workshops, and the open public consultation.

The EU's technology and ecosystem profile remains concentrated in automotive, power, analogue, and sensor segments, with limited exposure to leading-edge logic manufacturing. Structural gaps persist in advanced packaging, substrates, and back-end manufacturing, resulting in continued reliance on non-EU facilities for critical stages of production. This dependence introduces additional logistics, coordination, and lead-time costs at the system level and reduces resilience to trade disruptions, even where offshoring remains cost-efficient for firms.

Current cybersecurity legislation, such as the Cyber Resilience Act, will ensure that semiconductor products placed on the European market meet common security requirements, which may favour European suppliers who have a long legacy of secure and trusted products.

([143]) Technopolis Group, Cloud and AI Study for DG CNECT, November 2025

([144]) IBS Global Semiconductor Industry Service, Semiconductor Market Analysis by Geographic Region May' 25.

Dependence on imported materials, specialty chemicals, and industrial gases remains largely unchanged. While supplier diversification and recycling mitigate some risks, exposure to geopolitically concentrated supply chains continues to add price volatility and compliance-related cost premia.

Overall, under BAU, public support measures are sufficient to sustain limited capacity expansion but insufficient to overcome Europe's structural cost and ecosystem disadvantages. As a result, the EU's relative position in global semiconductor manufacturing improves only marginally, with no significant convergence towards the cost, scale, or time-to-market performance of leading Asian ecosystems.

5.1.2.5 R&D&I leadership in the EU semiconductor industry

The EU sustains a high level of scientific excellence, supported by R&D at universities, companies, and strong Research and Technology Organisations. Yet, as set out in Section 5.2 of the Evaluation Report, this **research strength only partly translates into industrial innovation and manufacturing capacity**. The establishment of the cloud-based Virtual Design Platform, competence centres, and pilot lines gradually improves access to design tools, technology validation services, prototyping services, and multi-project wafer runs, especially for SMEs and start-ups.

However, systemic barriers remain in the form of late-stage financing gaps, fragmented governance, and dependency on non-EU foundries, which impede firms from scaling prototypes into commercial products, all confirmed by the public consultation ([145]). By 2030–2035, these constraints prevent the full realisation of the Chips Act's ambition to bridge the research–industry divide, with many promising actors unable to advance beyond TRL6–8. As a result, the EU's strong research base does not translate into a commensurate increase in domestic design activity or industrial scale-up.

5.1.3 Environmental impacts

Under a BAU scenario, until 2035, Europe's semiconductor industry expands while remaining one of the most environmentally sustainable manufacturing regions globally. Front-end capacity rises from 1.07 million wafer starts per month (wspm) in 2023 to around 1.69 million wspm by 2035 (≈ 20.28 million wspy), maintaining an 8-9 % share of global capacity, but with a lower emissions and resource-intensity profile than most competing regions, particularly East Asia.([146])([147]). Although absolute electricity demand more than doubles, Europe benefits from a cleaner and rapidly decarbonising power mix, higher penetration of renewable PPAs, and stronger efficiency standards than the US and Asian hubs, leading to a 20-25% reduction in emissions intensity by 2035.([148])([149]). In contrast to many Asian manufacturing clusters facing severe water scarcity and limited reuse, European

([145]) Annex 4 of the Impact Assessment.
([146]) World Fab Forecast | SEMI
([147]) Invisible emissions | Greenpeace
([148]) JRC. (2025). *EU's strengths and weaknesses in the global semiconductor sector (JRC141323).* Luxembourg: Publications Office of the European Union.
([149]) McKinsey & Company. (2025). *Semiconductors have a big opportunity—but barriers to scale remain.* McKinsey Global Institute.

fabs routinely achieve 75-85 % water recycling rates ([150]), supported by strict permitting and environmental impact assessments, even as total withdrawals reach ~218 million m³/year.

Emissions from fluorinated gases decline faster in the EU than in other regions due to an ambitious EU F-gas Regulation and quicker adoption of climate-friendly technologies ([151]). While total Scope 1 and 2 emissions still rise with capacity growth (to approximately 1.3-1.6 $MtCO_2e$ Scope 1 and 7.2-8.5 $MtCO_2e$ Scope 2, location-based) ([152]), European fabs operate under higher transparency, stricter environmental standards, and stronger integration of energy- and water-efficiency technologies than most global peers. Overall, compared with other semiconductor regions, **Europe positions itself as a front-runner in sustainable semiconductor manufacturing,** leveraging cleaner energy, world-leading equipment and chemical suppliers, and strong regulatory frameworks to combine industrial expansion with comparatively lower environmental impacts. ([153])

5.1.4 Social impacts

5.1.4.1 Jobs in the EU semiconductor industry

Under a BAU trajectory, employment in the EU semiconductor sector grows steadily but **remains structurally constrained by persistent skills shortages and uneven regional capacity**. Between 2025 and 2030, job creation is driven primarily by fabs and expansions already under construction, including those by Intel in Ireland; STMicroelectronics-GlobalFoundries in Crolles; ESMC, Infineon and GlobalFoundries in Dresden; and STMicroelectronics in Catania, as these projects transition from construction to steady production.

As discussed in Annex 4 Section 2.1, under current policies, skills constraints remain a limiting factor: according to a European Chips Skills Academy (ECSA) report, the sector is projected to add around 156,000 jobs by 2030 and face approximately 271,000 cumulative openings including replacement needs, while graduate inflows are expected to grow by around 1% per year, resulting in a projected annual shortfall of around 16,800 unfilled technical roles by 2030 thus limiting the extent to which announced investments translate into realised employment.([154]) Skills needs emerged also as a cross-cutting issue of participants in various workshops, interviews and in the open public consultation. It was also pointed out that semiconductor skills pipelines require decade-long investment horizons, yet relevant programmes operated on shorter budgetary cycles, limiting structural impact.([155])

This situation is expected to exacerbate should manufacturing capacity further increase beyond currently announced investments under the Chips Act. A factor that the ECSA study does not consider is the scaling up of European fabless start-ups with the commensurate

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([150]) SEMI. (2023). *Sustainability in the Semiconductor Manufacturing Supply Chain.* SEMI Global Update.
([151]) Fluorinated greenhouse gases - Climate Action
([152]) All calculations are presented in Annex 4.
([153]) Chip Production's Ecological Footprint: Mapping Climate and Environmental Impact
([154]) European Chips Skills Academy (ECSA), Decision Etudes & Conseil. (2024). *European semiconductor skills strategy 2024.* Luxembourg: Publications Office of the EU.
([155]) Annex 2 of the Impact Assessment.

demand for skilled chip designers, a scarce resource, this would result in, or the impact that the ongoing AI boom will have on the semiconductor manufacturing equipment industry in Europe.

5.1.5 Governance

5.1.5.1 Supply chain monitoring

Under the BAU scenario, the governance of the supply chain remains constrained by **insufficient insight into supply chain resilience**, as the Commission continues to rely primarily on voluntary information sharing (Arts. 19 and 20 of the Chips Act) and crisis-specific mandatory data collection (Art 25). The stakeholder consultation also confirms that Pillar III has only partially met its objectives. ([156]) However, in a pre-crisis stage, a comprehensive understanding of the market is essential. Unlike the proactive and broader provisions established in the US under the Trade Act,([157]) which can mandate data gathering for national security purposes, the EU framework still lacks sufficient legal leverage to compel industrial stakeholders to share granular data on stock levels, suppliers, and customers outside of officially declared emergencies. The evaluation confirms these constraints: crisis coordination and monitoring mechanisms remain underdeveloped, and there are no means to monitor and anticipate supply chain disruptions in real time. ([158])

The existing provisions for early warning indicators and the crisis toolbox also remain reactive and continue to function largely as activation mechanisms for crises rather than drivers of structural preparedness. While larger companies may increase their risk anticipation and mitigation efforts, significant parts of the European semiconductor ecosystem remain highly vulnerable to geopolitical tensions and supply interruptions. Without new policy intervention, this results in persistent blind spots that prevent the Union to gain a deep real-time understanding of the value chain, to anticipate disruptions to the supply chain before they escalate, to design effective policy responses, to direct investment and to coordinate Member State actions aimed at enhancing supply chain resilience.

Under the BAU scenario, the current Chips Act provides an initial stable and Union-wide framework for the monitoring of parts of the European semiconductor value chain. However, while certain segments are beginning to benefit from ongoing investments and coordination structures, these developments remain partial and have not yet generated a step change in the EU's overall position. Ecosystem resilience improves but dependencies remain throughout the value chain: production capacity grows but is expected to stagnate in the long term; manufacturing sophistication advances incrementally but does not shift the EU into the leading edge; and the Union remains unable to capitalise on its excellent research capacity.

([156]) Annex 2 of the Impact Assessment.
([157]) Trade Act of 1974, Pub. L. No. 93-618, 88 Stat. 1978 (1975).
([158]) See Evaluation of the Chips Act

5.2 Description of the policy options

Policy options for **Chips Act 2.0** were developed based on alternative approaches to industrial and innovation policy. The options are differentiated by the extent to which they rely on two distinct industrial policy models:

- The **horizontal ("market-enabling") policy approach (PO1)** focuses on improving overall framework conditions through increased support for research, development and innovation, investment in skills, and the creation of a favourable investment environment**, without introducing additional Union-level funding for mass-scale manufacturing and design, notably for AI chips**.
- The **vertical ("proactive") industrial policy approach (PO2)** builds on the horizontal measures but complements them with targeted financial interventions, notably through **Strategic Projects** supported under the proposed **European Competitiveness Fund**. This approach builds on the European technological assets supported under of the first Chips Act, in particular pilot lines, and translate them into industrial deployment. By introducing a clear EU-level dimension to funding industrial projects and enabling cross-border, value-chain-wide investments, this approach aims to reduce fragmentation while strengthening Europe's competitiveness, resilience and technological sovereignty.

Policy options should be read cumulatively, as each subsequent option includes all the measures of the previous one and adds further elements:

5.2.1 Policy Option 0: "The status quo/baseline scenario"

This would involve the continued implementation of the current Chips Act without any modification. It will maintain the existing R&D&I programme under Pillar I and maintain the same approach to supporting investments through State aid (using the "first-of-a-kind" framework through the existing State aid rules) with no additional Union or Member State budget under Pillar II. Under Pillar III, it will also maintain the current crisis response mechanism, which operates with depends on a voluntary data-gathering regime (except in a crisis). This policy option will not include any policy measures going beyond the scope of the existing Chips Act.

5.2.2 Policy Option 1: "Measures that focus on the framework conditions"

In line with the **horizontal approach** to industrial policy, this policy option is based on measures focusing on framework conditions (permitting standards, energy supply, infrastructure, labour skills, etc.) alongside R&D&I interventions.

5.2.2.1 PM1: Increased R&D&I support through the Chips JU

This measure will build on the R&D&I activities under the Chips Act and go further by increasing support in line with the possibilities of the digital windows of the proposed 10th Framework Programme and the European Competitiveness Fund to maintain European leadership in semiconductor research and support the transition from the 'lab to the fab'.

The focus now shall be on more industrially relevant activities that have a clear path to industrialisation. This shall especially be the case when it comes to pilot lines, which in the

first Chips Act are deployed by Research and Technology Organisations. In their next iteration, industrial partners shall be expected to exploit their results.

Sub-measures here could include new or expanded pilot lines, support for research and deployment focusing on the production of quantum chips, doubling down on the support provided via the Design Platform, a renewed Chips Fund 2.0 and additional funding for R&D&I activities under the successor of the Chips JU. Areas of the new pilot lines could include smart glasses, non-volatile memories, 3D integration. The proposed European Competitiveness Fund is expected to provide novel means to support activities with EU direct management funds that are more attuned to industrial deployment.

5.2.2.2 PM2: Clarification of the scope of 'first-of-a-kind'

The proposed clarification of the definition of first-of-a-kind (FOAK) shall serve as a more detailed explanation, intended to remove ambiguity and ensure that the entire semiconductor value chain is consistently covered. Under the current definition, the scope of FOAK could have been interpreted by Member States and stakeholders unevenly, *de facto* limiting support to certain segments of semiconductor manufacturing due to the lack of clarity for more upstream and downstream activities that are equally critical to the semiconductor industry. This policy measure builds on this architecture by further clarifying the scope of the first-of-a-kind (FOAK) framework.

Therefore, **PM2** provides for the **clarification of the first-of-a-kind scope**, specifically incorporating elements to increase the focus on **resilience within the FOAK assessment**:

- The **first-of-a-kind scope** is clarified to explicitly include the **entire semiconductor value chain, by clarifying that FOAK** does not only focus on FOAK **"facilities"** but on **"initiatives,"** to clarify that FOAK is not only focused on new or substantially upgraded semiconductor manufacturing facilities with an IDM or foundry model, but may also cover other projects in the value chain such as materials or equipment.
- The FOAK definition is clarified to **explicitly cover innovative investments that provide resilience in the semiconductor supply chain**, including for mature technology nodes. **Underrepresented facilities** that address **chokepoints in the supply chain** (such as **mainstream or packaging**) could qualify as **first-of-a-kind** if they strengthen the Union's resilience. The **Nexperia case** demonstrates that these facilities carry a critical **economic and resilience dimension** for the Union. It may be the case that several parallel projects are recognised as first-of-a-kind, as long as it can be proven that those projects do not crowd out existing or planned private activities or create overcapacity. Hence, in light of economic security considerations, certain manufacturing investments that are critical for reducing dependencies on third countries or third country entities may warrant support where, next to innovation, resilience is an element to take into account in the assessment and the investment contributes to the security of supply.

Clarifying the scope of FOAK to ensure projects with a clear resilience dimension can fall within the FOAK definition would enhance coherence with EU objectives such as economic security, while remaining consistent with State aid and competition law principles.

While the mentioned activities are already covered by the current framework based on the Commission's practice, stakeholder feedback indicates that this is not always sufficiently clear in practice, which results in hesitation by Member States to pursue such projects.

Therefore, the clarified FOAK scope would improve legal certainty and reduce interpretative divergence.

5.2.2.3 PM3: Fast-track permitting procedures

Fast-track permitting procedures will build on the proposal for the 'Regulation on speeding up environmental assessment'[159] and potential other upcoming legislation. In that respect, the Chips Act 2.0 will be adopting similar provisions to the Industrial Accelerator Act (IAA) proposal for semiconductor-related facilities, as semiconductors do not fall under the scope of the proposed IAA ([160]).

5.2.2.4 PM4: European Semiconductor Regions of Excellence Label

The European **Semiconductor Regions of Excellence seal** would serve as a soft measure giving recognition to regions implementing a framework of enabling policies. This seal would recognise the key role that regions play in supporting the semiconductor industry. The criteria for granting this seal includes **regional measures to support infrastructure, value-chain development** and **skills**, the establishment of a **one-stop-shop** for all regulatory approvals, **designated land for industrial deployment**, **single-points of contact for administrative processes** and other framework conditions.

The seal would recognise regions that have direct measures in place to support the semiconductor value chain and attract investments, and aims to encourage additional regions to also take supportive measures. A network of labelled regions would be supported to exchange good practices.

The exact requirements for such a seal would be set out in a delegated act. Regions' adherence to this measure would be monitored by the Commission.

5.2.2.5 PM5: Establishment of a Business-to-business Semiconductor Supply Chain Platform

A **Business-to-Business Platform** ("the Platform") would enhance supply chain transparency and resilience through an industry-led process. The Platform would operate as a secure **digital twin of the supply chain**, enabling participating firms to upload relevant information in a secure environment. Companies would benefit from aggregated insights on supply chain risks, thus supporting internal resilience-building and reducing their own market-information costs. Companies would benefit directly from sharing their data by gaining access to aggregated insights on the overall supply chain. These insights should encourage undertakings to take proactive actions to enhance their supply chain resilience without public sector intervention. For the Commission, a proactive and resilient private sector ensures a lower risk

[159] COM(295) 984 final | Regulation on speeding-up environmental assessments
[160] Industrial Accelerator Act - Internal Market, Industry, Entrepreneurship and SMEs

of activation of the crisis stage and deployment of the emergency toolbox. The Commission would provide initial support for establishing the platform and cover the setup costs through a competitive call. The participating companies should decide on the governance structure of the Platform and designate its legal representative, while the financing model of the Platform should be thought out by the beneficiary of the call. The platform should eventually be self-sustaining.

Participation in the Platform will be voluntary, except for Strategic Projects and Semiconductor Technologies Facilities, which will be required to join as a precondition for receiving public funding. As envisaged by the Data Governance Act, the Platform will operate in a secure processing environment, respecting all Union legislation including EU antitrust compliance. In the event of a pre-crisis, as a preventative action, previously discussed with and advised on by the European Semiconductor Board, the Commission would have the possibility to request aggregate information from the Platform.

5.2.2.6 PM6: Information requests for aggregate data sent to the Platform in pre-crisis stage

In situations where an alert is triggered ([161]), the Commission could send a request for information to undertakings. This measure enhances the information available to public authorities outside the formal crisis stage. It follows a **two-step approach**:

- Working closely with the European Semiconductor Board, the Commission could request information to the Platform, supported where possible by aggregated, non-sensitive data from the Platform. The request for information should be sent to the legal representative of the Platform, state its legal basis, purpose, be limited to what is necessary and proportionate in terms of volume of the data and frequency of access to the data requested, have regard for the legitimate aims of the Platform and set out the time limit within which the information is to be provided, and possible penalties according to Article 33 of the Chips Act.
- If the answer is not sufficiently comprehensive, the Commission may issue mandatory requests for information to individual companies that are not participating in the Platform. These requests for information shall state the legal basis and purpose of the request, be limited to what is necessary and be proportionate in terms of volume of the data and frequency of access to the data requested, set out the time limit within which the information is to be provided and possible penalties for incorrect, incomplete or misleading information.

Where the Commission becomes aware of a risk of serious disruption in the supply of semiconductors, or has concrete and reliable information of any other relevant risk factor or event materialising, it shall without undue delay carry out the preventive actions set out in Article 22 of the ECA.

([161]) As set out in Article 22 paragraph 2 of the Chips Act.

5.2.2.7 PM7: Increased investment in skills initiatives

This measure would promote coordination and investment in skills for the European semiconductor sector via **targeted upskilling and reskilling programmes** to support the rapid adaptation of the existing workforce in the framework of the Skills Partnership for Microelectronics under the Pact for Skills ([162]). Members of the Pact already have access to data on upskilling and reskilling needs, advice on relevant funding instruments to support life-long learning in their regions and countries, and partnership opportunities within a growing community. Here, up-skilling and re-skilling initiatives focus not only on semiconductor firms but also the broader value chain.

These activities would be intensified under Chips Act 2.0 and also be supported via actions under FP10 as implemented by the successor to the Chips JU whose tripartite governance involving the Union, Member States and industry enables the definition of initiatives that respond to different realities in Member States, regions and segments of the semiconductor industry.

5.2.3 Policy Option 2: "Strategic sovereignty"

This policy option adds a more vertical approach to industrial policy under the revised Chips Act, while also including the policy measures listed above (from PM1 to PM7).

5.2.3.1 PM8: Strategic Projects

This measure would adapt the Chips Act to the new realities and possibilities provided by the upcoming Multiannual Financial Framework, particularly the proposed European Competitiveness Fund, which will potentially allow direct management funds to support Strategic Projects ([163]) focused on industrial deployment. Strategic Projects are an answer to the specific economic conditions in the semiconductor industry characterized by large investment volumes and high fixed costs, ecosystem clustering, and path dependencies. Such projects would be developed by fostering a **mix of public and private investment,** including potential additional public investments by Member States through a combination with the concept of FOAK. This would enable EU-level supported investment across the semiconductor value chain through the proposed European Competitiveness Fund. It would complement the current Pillar II framework by introducing direct EU funding, thus increasing the overall scale of public investment, strengthening the cross-border dimension through the integration of manufacturing, design, and supply chain activities, and placing greater emphasis on strategic autonomy and technological sovereignty. Strategic Projects would allow for cross-border, value-chain wide investment that would seek to create synergies across the European semiconductor ecosystem. They would also aim to better integrate SMEs and SMCs along the value chain. The approach is also in line with the **first recommendation of Draghi report** for a "*centralised EU budgetary allocation dedicated to semiconductors, allowing Member States' co-investment on priority initiatives and industrial projects of high EU added value."*

([162]) Microelectronics | Pact for Skills
([163]) Article 8 of the European Competitiveness Fund proposal.

In deploying Strategic Projects, a public-private partnership funding framework **similar to the one used for the AI Gigafactories** could be used, mixing grants (co-financed by the EU and Member States in compliance with State aid rules) and private investments from industry, which would in turn be supported by the European Investment Bank and the European Investment Fund, as well as other sources of public and private investment funds ([164]).

By structuring the investment through a mix of grants and financial instruments (equity, loans, guarantees), the Union could aim to mobilise both public and private sector participation while de-risking capital-intensive projects. When it comes to grants, both EU and Member States participation could be envisaged with a variable level of contribution between the EU and Member States, depending on the Strategic Project.

To qualify, a project must comply with certain criteria:

(i) deliver clear EU added value and support European priorities;
(ii) have a cross-border dimension;
(iii) strengthen the resilience, indispensability, and prosperity of Europe's semiconductor ecosystem;
(iv) contribute meaningfully to Europe's technological sovereignty and leadership.

Strategic Projects would be paired with demand-side measures (PM9, PM10) to increase demand predictability and therefore improve utilisation rates, which is a critical factor for the competitiveness of facilities with high fixed-costs.

Strategic Projects are explicitly designed as cross-border value-chain investments creating spillovers that are economically durable: skills development, local supplier-customer engagement, shorter innovation cycles, higher throughput. These effects improve productivity and reduce costs with a flywheel effect supporting growth across the entire EU ecosystem.

5.2.3.2 PM9: Innovation procurement and support for grand challenges

5.2.3.2.1 Innovation procurement

To contribute to the sustainability and viability of Strategic Projects (PM8), the revised Chips Act will make demand stimulation through **innovation procurement** (pre-commercial procurement and procurement of innovative solutions) an objective under Pillar I of the Chips Act. This objective will complement the Chips Fund in scaling up start-ups in Europe. A first application of this principle could be the deployment of AI chips designed in the EU. This measure would target start-ups and SMEs that are scaling up and would be applicable to firms across the semiconductor value chain.

Under PM9, Pre-Commercial Procurement (PCP) ([165]) could be used to create open EU-wide competition for prototype development and testing, with R&D contracts up to TRL 8. These

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([164])https://www.eib.org/en/press/all/2025-491-eib-group-and-european-commission-join-forces-to-finance-ai-gigafactories

[165] European Commission. *Pre-commercial procurement: Driving innovation to ensure sustainable high quality public services in Europe*. Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions. COM(2007) 799 final. Brussels:

contracts could be awarded in phases, with suppliers selected based on performance and EU added value. Where results meet the set requirements, public buyers can purchase and deploy the best-performing solutions taking the obligation of current public procurement directives to organise a competitive and transparent procedure into consideration ([166]). The involvement and stimulation of the private sector as a buyer of European innovation is also foreseen through grants for procurement.

The first foreseen application of this measure is AI chips and systems for compute infrastructure, where procurement can be managed by European AI Factories. Deployment would include prototype orders, benchmarking in AI Factory environments, and if successful, follow-on procurement. The same logic could be repeated at a later stage also with AI Gigafactories, with broader ambitions for energy-efficient compute solutions built around European technology.

Similar approaches can be followed in tandem with "grand" challenges for other domains depending on strategic priorities:

- Automotive / autonomous driving processors: safety-critical compute, sensor fusion, AI inference
- Secure processors: e.g. trusted CPU platforms for public sector and critical infrastructure
- Ultra-energy-efficient computing: low-power architectures for edge, industrial, robotics, drones.
- Telecom and network infrastructure chips: secure connectivity, RAN acceleration, network processing
- Defence, space and secure communications: high-reliability and sovereignty-critical chips
- Key enabling tools and equipment where Europe has strong capabilities but limited first deployments: e.g. advanced packaging test/inspection, metrology, design automation components, verification toolchains.

The key target beneficiaries of the measure would be EU-based start-ups/SMEs and scale-ups, particularly fabless companies, as well as public buyers and strategic end-user industry sectors, that will benefit from the delivered results. Further, depending on the focus of the call, other key value-chain actors, such as equipment, IP, tools, packaging and testing, and the wider EU semiconductor ecosystem.

5.2.3.2.2 Grand challenges

The scope of grand challenges is the bridging of the gap between pilot line results and industrial adoption by structuring close collaboration between pilot lines and Research and Technology Organisations, start-ups and SMEs, and end-user industries (automotive, industrial, telecom, defence, healthcare, datacentres). The focus of this measure will be on concrete technology tracks such as advanced packaging/chiplets (2.5D/3D), silicon photonics,

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European Commission, 2007. Available at: https://eur-lex.europa.eu/LexUriServ/LexUriServ.do?uri=COM:2007:0799:FIN:EN:PDF.

[166] Directive 2014/24/EU on public procurement. This regulatory framework is under revision: Revision of the Public Procurement Directives | Public Buyers Community

low-power edge-AI platforms, power semiconductors (SiC/GaN) and secure hardware (trusted chips). The model shall be entrenched in application-driven programmes with users in domains such as autonomous driving hardware, robotics, and wearables (e.g. smart glasses), by accelerating prototyping, qualification and integration into real products with clear market value.

5.2.3.3 PM10: Recommend a security of supply declaration for semiconductors in public procurement

This measure would apply to public procurement, auctions and other forms of public intervention involving semiconductors or semiconductor-enabled systems used in critical and strategic sectors within the Union in scope of Annexes I and II of Directive (EU) 2022/2555 (NIS2). It would be a soft policy measure with the aim to increase supply chain transparency and the share of semiconductors supplied by EU undertakings (domestic) or undertakings from countries which can provide an equivalent level of supply chain reliability (equivalent), for instance via the signature of free-trade agreements, participation in multilateral framework such as the General Procurement Agreement or strategic partnerships on semiconductor supply.

Concretely, PM10 would allow public procurement authorities to request from tenderers a supply chain declaration analysing the provenance of semiconductors in the tendered products, outlining their supply chain resilience strategy, in particular with regards to dual sourcing. The declaration would also need to assess the quota of semiconductors supplied from domestic undertakings or equivalent. The public procurement authorities may use the supply chain resilience strategy as outlined in the declaration, and the quota of domestic or equivalent semiconductor suppliers, as award criteria along with price.

The proposed PM10 would be complementary and without prejudice to the "Security of ICT Supply chains" framework laid out in the Commission's proposal for a Cybersecurity Act 2 (CSA2). While the CSA2 proposal focuses on the cybersecurity aspect, PM10 would address the security of supply aspect, targeting a persistent demand-side market failure that undervalues long-term resilience in procurement decisions, particularly where price-based competition risks favouring subsidised and potentially unreliable suppliers. The limited transparency of long supply chains risks exposing critical sectors in the Union to dangerous dependencies, which could grow unnoticed and then create disruptions as happened in the Nexperia case.

The primary addressees of this measure are public authorities and operators in critical sectors, which would benefit from more secure, resilient and trustworthy semiconductor supply chains. Semiconductor manufacturers from the European Union and from equivalent countries would benefit from reinforced market access and investment certainty. Ultimately, end users and citizens would benefit from improved security, reliability and continuity of essential services and infrastructure across the Union.

5.2.4 Overview of policy options

An overview of the policy options in line with the three-pillar structure of the Chips Act is provided in the table below. The economic, social, and environmental impacts of these

options are assessed in Chapter 6 of this impact assessment, while a comparison of the options is provided in Chapter 7 of this report.

Pillars	***Policy Option 0: the baseline/ business as usual scenario***	***Policy Option 1: Measures that focus on the framework conditions***	***Policy Option 2: Strategic sovereignty (Includes measures of PO1 and additional measures)***
Pillar I: The 'Chips for Europe' Initiative	Continue the existing R&D&I program in the Chips JU.	**PM1:** Increased R&D&I support through the Chips JU.	**PM1:** Increased R&D&I support through Chips JU. **PM9:** Innovation procurement and support for grand challenges based on procurement (PCP). Lab-to-fab industrial accelerators
Pillar II: Security of Supply and Resilience	The current "first-of-a-kind" framework.	**PM2: Clarification of FOAK's s**cope to include the value chain and its relationship with IPF, OEF. Clarification of FOAK to highlight security of supply and resilience aspects	**PM8: Strategic Projects** stemming from the **ECF** proposal. **PM2**: Clarification of FOAK's scope to include the value chain and its relationship with IPF, OEF and Strategic Projects. Clarification of FOAK to highlight security of supply and resilience aspects
Pillar III: Monitoring and Crisis Response	The existing crisis response mechanism based on a voluntary data-gathering regime.	**PM5:** Establish a Business-to-business semiconductor supply chain Platform. **PM6:** Information requests for aggregate data sent to the Platform in pre -crisis stage	**PM5:** Establish a Business-to-business semiconductor supply chain Platform. **PM6:** information requests for aggregate data sent to the Platform in pre -crisis stage
Other interventions	No additional policy measures.	**PM4:** The European Semiconductor Regions of Excellence seal **PM7:** Increased investment in skills initiatives **PM3:** Shorter and streamlined permitting processes.	**PM7:** Increased investment in skills initiatives **PM3:** Shorter and streamlined permitting processes. **PM10: Recommend a security of supply declaration** for semiconductors in public procurement

5.3 Options discarded at an early stage

Current semiconductor supply chains remain highly geographically concentrated, with several essential technologies sourced from less trustworthy third countries([167]). This introduces systemic vulnerabilities: single-point supply chain failures, coercive economic practices, long-lead disruptions and risks to public safety. Certain critical sectors cannot operate effectively without a regular, trusted, and verifiable supply of advanced semiconductor components.

([167]) Special report 12/2025 - The EU's strategy for microchips

To materially reduce strategic dependencies, one considered policy response – "trusted chips preference" - was to establish legally binding obligations to use trusted chips for operators of critical infrastructure as listed in Annex 4 of the Chips Act. This option would go beyond procurement preference.

Furthermore, direct mandatory information-request provisions for all companies were considered that would have enabled the Commission, **under all circumstances**, to obtain not only qualitative assessments and aggregate data, **but also granular, company-level information**, **including business-confidential data where necessary**.

However, this policy option of "trusted chips preference" and "mandatory information requests" was discarded due to overlap with existing legislative acts, such as in the area of cybersecurity and ongoing revisions of the cybersecurity framework. Furthermore, this option could impact the competitiveness of EU user industries.

6 WHAT ARE THE IMPACTS OF THE POLICY OPTIONS?

The impacts of the different policy options are assessed below based on the methodology set out in Annex 4, the results of the open public consultation and Call for Evidence summarised in Annex 2, analysis gained from over 20 targeted workshops with specific stakeholders' groups, desk research and external studies. Only the relevant types of impacts affecting each Pillar are assessed. Overall, the initiative is not expected to have any impact on fundamental rights. The baseline scenario, outlined in Section 4.1 describes the implications and costs associated with taking no further action.

6.1 PO1 "MEASURES THAT FOCUS ON IMPROVING THE FRAMEWORK CONDITIONS"

Policy Option 1 takes a non-interventionist approach to strengthening the EU's semiconductor ecosystem. Unlike Policy Option 2, it provides no additional Union funding and introduces no additional direct financial support for manufacturing or supply chain resilience. Instead, it focuses on improving framework conditions and horizontal support measures.

6.1.1 Economic impacts

6.1.1.1 Impacts on EU semiconductor firms' revenues

Semiconductor firm revenues

For EU-headquartered semiconductor firms, **PO1** would largely maintain the status quo. However, through **PM3,** the policy option would ease the business environment for the semiconductor industry, through simplification efforts via shorter permitting times for the deployment of manufacturing capacity. This measure would allow the Union to tackle the external competitiveness issues that it faces as set out in Figure 12 of **PD2,** as permitting and design timelines differ significantly between Taiwan, Southeast Asia and the EU. Analysis in Annex 3 shows how European firms stand to save up to EUR 625 million in administrative costs if permitting delays are addressed as set out in **PM3**.

A 2025 study by the OECD has shown that high regulatory burdens and compliance costs are "a factor associated with weaker labour productivity growth and business dynamism" ([168]). Reducing these burdens would enable European firms to shift scarce resources to more productive activities, which would in turn support an increase in revenue growth.

This would be complemented by the European Semiconductor Regions of Excellence seal (**PM4**), through which participating regions would have deployed enabling initiatives in the areas of skills, infrastructure and administrative processes, thus supporting the reduction of administrative burdens and supporting productivity growth. Its impact will vary by regional baseline and cannot yet be quantified, as requirements will be set by delegated act.

Intensified skilling and re-skilling initiatives (**PM7**) support revenue growth indirectly by easing skills shortages that constrain productivity, ramp-up and time-to-market (see section 5.1.3.3).

In essence, **PO1** is expected to have a limited impact on the market share trajectories of EU-headquartered semiconductor firms manufacturing in Europe. While **PM3** would marginally improve operating conditions through faster permitting and administrative simplification, these measures primarily reduce friction rather than materially strengthening firms' competitive position. Similarly, the European Semiconductor Regions of Excellence seal under **PM4** would provide visibility and signal regional commitment, but in the absence of differentiated financial incentives, its effect on investment decisions and capacity expansion is likely to remain modest. **PM7.** As a result, **PO1** would broadly preserve existing market dynamics, supporting continuity rather than driving a step-change in the global competitiveness or market share growth of EU semiconductor firms.

6.1.1.2 Semiconductor value chain

PM2 would clarify the scope of FOAK to include the wider semiconductor value chain. Here, the new FOAK definition would concentrate on clearly defined strategic priorities where EU action is needed and can deliver the highest benefit in terms of security of supply and technological leadership as set out in **PM2**. This clarification will enable Member States to provide a more compelling case to semiconductor firms investing in the Union, anchoring higher value-added activities within the Union and support the sustained expansion of the European semiconductor value chain, rather than isolated capacity growth. This shall in turn support more competitive firms which may increase revenues. At the same time, such a measure could potentially fragment Member State's budgets to a broader number of firms, thus risking less concentrated support.

The Semiconductor Regions of Excellence seal (**PM4**) would also introduce a regional dimension to the Chips Act by encouraging regions to support the semiconductor value chain through for example infrastructure investment and skills initiatives. Since the seal will recognise regions who have direct measures supporting the value chain, it may also encourage regions that do not host semiconductor firms directly but are home to firms that contribute to

([168]) OECD (2025), OECD Economic Outlook, Volume 2025 Issue 2: Resilient Growth but with Increasing Fragilities, OECD Publishing, Paris, https://doi.org/10.1787/9f653ca1-en.

the broader value chain, to also focus on the strengthening of said ecosystem. This shall be complemented by more comprehensive skills initiatives tackling both semiconductor firms but also the value chain under **PM7** which will have similar impacts as described above for semiconductor firms.

Therefore, Policy Option 1 would reinforce the EU's semiconductor ecosystem along existing strengths, but without much coordination for concerted European action on value chain resilience. **Nevertheless, through a clarification of the FOAK definition, a larger share of planned projects would be expected to proceed compared with the baseline scenario (BAU).**

6.1.1.3 Impacts on manufacturing capacity

Policy Option 1 could moderately increase Europe's attractiveness for investment and enable a larger number of potential projects to be realised when compared with BAU but this would largely depend on market dynamics and Member State and regional budgets.

Available evidence suggests that the EU's expansion potential currently lies in mature and application-specific technology nodes, where it already has a significant foothold. Reducing regulatory burdens in permitting (**PM3**) and alleviating infrastructure bottlenecks (**PD2**) through the Semiconductor Regions of Excellence label (**PM4**) would increase the likelihood that planned projects in these segments materialise, thereby enabling incremental increases in production over time. These effects would occur against the backdrop of the EU's comparatively less favourable business environment. By setting voluntary standards for regions to support their local semiconductor industry and streamline regulatory compliance requirements, the Semiconductor Regions of Excellence label would reduce administrative overhead for industry stakeholders.

As set out above and in Annex 3, in Taiwan, these phases typically take between 6 and 13 months, whereas in the EU they usually require 16 to 18 months ([169]). This implies that permitting and design in the EU are approximately 3 to 10 months longer than in Taiwan. Using midpoint estimates, ([170]) the average amounts **to roughly 7.5 months additional time**. As set out in Annex 3, the assumption that each year of delay adds around 5 % of total project value ([171]) implies an additional cost equivalent to 3.125 % of overall investment. Concretely, for a representative EUR 20 billion advanced semiconductor fabrication plant, this corresponds to **roughly EUR 625 million** in additional expenditure. Therefore, a reduction in permitting times (**PM3**) would substantially improve Europe's competitiveness and in turn increase the viability of setting up manufacturing facilities in the EU.

However, the capacity of **PO1** to generate substantial new manufacturing capacity in leading edge technologies, will largely depend on organic growth and the capacity of Member States to support such investments through State aid. The more likely outcome is that **PO1** would

([169]) see Figure 12 - Average duration of projects for building wafer fabs
([170]) Around 9.5 months for Taiwan and 17 months for the EU
([171]) https://www.csis.org/analysis/streamlining-permitting-process-fab-construction

consolidate the EU's existing strengths in mature and application-specific nodes, support equipment upgrades in current facilities and reduce critical dependencies.

6.1.1.4 Impacts on demand

No demand stimulation measures are foreseen under Policy Option 1 and therefore no change in impact when compared to the baseline is expected.

6.1.1.5 Impacts on the cost (price) competitiveness of the EU industry.

Under BAU, the EU remains the highest-cost manufacturing location among major regions.([172]) **PO1 would not significantly close this structural gap**, as it mainly stems from capital-intensive investment conditions beyond the scope of this option. However, as highlighted by the Draghi report, by improving predictability, reducing regulatory complexity and streamlining permitting procedures, **PO1 could enhance competitiveness and support incremental productivity gains.**

On capital costs, faster permitting as set out in **PM3** as well as better-coordinated infrastructure planning and clearer regulatory requirements under **PM4** would reduce delays and contingencies that, as discussed in **PD2**, currently inflate investment costs through extended construction timelines and higher financing costs. Under Policy Option 1, smoother project execution would lower risk premia and help keep projects within budget, **particularly in Semiconductor Regions of Excellence** whose infrastructure and procedures are suitably adapted**.**

A clarified FOAK approach (**PM2**) would give Member States greater flexibility to support the entire value chain and thus support European industry in overcoming the cost constraints discussed in **PD2** due to localisation effects that lower logistics costs, reduce supply-chain vulnerabilities, and instil co-development.([173])

Other costs such as energy and labour costs are largely shaped by broader market conditions and would not be affected by this option. However, investments in skills (**PM7**) and more predictable framework conditions would raise labour productivity, support smoother ramp-up and enhance yields. By easing skills shortages, improving the general investment conditions and governance challenges, firms could reduce downtime, improve throughput and better leverage automation.

In these segments, **modest reductions in effective capital and operating costs**, combined with more reliable project delivery, **would lower risk margins than under BAU.** While the PO1 would strengthen the competitiveness of EU suppliers in automotive, industrial and power-electronics markets, where customers value cost efficiency and supply reliability. The effectiveness of accelerated permitting and streamlined FOAK will depend on Member

([172]) Benchmarking shows that production costs in the US are roughly 16% lower, while costs in leading Asian ecosystems can be up to 50% lower.
([173]) Co-development advantages include faster process co-optimisations and joint research activities that are common in dense ecosystems.

States' implementation capacity, which may produce uneven gains and potentially favour incumbents.

6.1.1.6 Impacts on public budget

Overall, the budgetary impact on EU, national and regional budgets would remain moderate compared with the existing Chips Act envelope.

At **Union level**, the main budget effects stem from increased R&D&I commitments within the the next MFF (2028–2034), notably through FP10 and the digital window of the proposed ECF. Support would focus on research, pilot lines and innovation activities implemented through existing instruments. Skills-related spending would increase relative to BAU, subject to availability of budget under the next MFF, and would be channelled through established funding streams. All this is subject to agreement on the next MFF, its programmes, and allocation of budgets from programmes to actions described here. This document does not alter or circumvent the design and architecture set out in the Commission's proposal on the MFF 2028–2034, nor does it pre-empt its implementation.

Administrative and coordination costs for establishing the Business-to-business **Semiconductor Supply Chain Platform (PM5)** are estimated at around **EUR 70 million.** These figures are based on an analysis of comparable data infrastructures such as CATENA-X.([174]) Implementation would also require approximately **six FTEs** within the Commission to gather, maintain and analyse data. These resources are necessary to anticipate disruptions, coordinate preparedness measures and ensure the effective functioning of the monitoring mechanism under Policy Option 1.

For Member States([175]), a clarified FOAK definition **(PM2)** would facilitate public support for semiconductor investments. This could increase national spending when compared with BAU, although the magnitude would depend on national priorities and fiscal headroom.

6.1.1.7 Impacts on R&D and innovation ecosystem

PO1 is expected to generate positive impacts on European R&D activity within the semiconductor ecosystem and related sectors through increased funding (**PM1**) via the proposed FP10 and ECF. The consultation process highlighted design capabilities as a recurrent priority, including support for fabless actors, open-source architectures and processor development. Under **PO1**, these priorities would primarily be addressed through reinforced Pillar I instruments under **PM1** (pilot lines, competence centres, quantum, design support and the Chips Fund 2.0), improving technology maturity and knowledge diffusion but with limited direct links to industrial-scale deployment. This additional support would also strengthen the scientific and technological capabilities of universities and Research and

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([174]) Delivered! 5 Stars! Catena-X: A 3-year, EUR 250 million software start-up success | DIH

([175]) It is not possible to quantify the potential increase in national expenditure, as this would depend on the specific form of simplification introduced, the fiscal space and policy priorities of individual Member States, and their willingness to expand or redesign national schemes. While streamlined procedures could reduce administrative costs and may lead to higher demand for support from firms, any resulting increase in national spending would remain uncertain and cannot be reliably estimated ex ante.

Technology Organisations. A secondary, indirect effect may result from reinforced complementary national actions since higher EU-level investment, that is contingent on co-funding, could incentivise Member States to increase their own R&D efforts in order to leverage synergies and maintain competitiveness. Such a dynamic could further boost the EU's capacity to advance semiconductor research and innovation.

Technology transfer and knowledge spillovers are likely to intensify as a consequence of increased R&D activity. The semiconductor sector already exhibits strong linkages between academia and industry, and existing Chips Act projects have established cooperation structures that reduce barriers to knowledge exchange. Enhanced collaboration should therefore facilitate the diffusion of scientific and technical know-how, including from foreign firms expanding their activities in the EU to domestic enterprises and universities.

The funding of **new actions on R&D&I (revised Pillar 1)** in Chips Act 2 will depend on the whether the digital windows of the proposed FP10 and the ECF are of sufficient size and scale to maintain European leadership in semiconductor research and support the industrialisation from the 'lab to the fab'. Since it is expected that the Chips JU will serve as the prime vehicle for the deployment of this funding, the modalities of how this R&D&I support will be deployed will be elaborated **in the upcoming policymaking process related to the follow-up legislation to Council Regulation 2021/2085** establishing Joint Undertakings.

When it comes to the impact of a renewed Chips Fund 2.0 in the next Chips Act, one can consider the outcomes of the current Chips Fund, which is implemented through the EIC accelerator and Invest EU. The Chips Fund has led to a total public investment of EUR 425 million and has resulted in the funding of 55 semiconductor and quantum startups, leveraging an average of EUR 3.8 of private investments for each Euro of equity investment from public funding.

6.1.1.8 Impacts on SME/start-up ecosystem

The **lab-to-fab gap** is widely recognised as a key barrier to start-up dynamism in the European semiconductor ecosystem. However, underlying drivers of this gap, such as limited venture capital and administrative burdens, reflect long-standing structural challenges for European start-ups. These issues fall beyond the scope of the Chips Act and require broader action. SMEs often face higher barriers to entry in Chips Act instruments, as application processes impose disproportionate administrative and compliance costs compared with larger firms.

Policy Option 1 is expected to generate only modest improvements for the start-up and SME ecosystem. Start-ups and SMEs would benefit indirectly from an improved regulatory framework as well as potential technology transfer and financial support from the aforementioned intensified R&D&I activities.

6.1.2 Environmental impacts

Under PO1, the estimated increase in environmental impact is moderate and reflects normal industry developments associated with capacity expansion. Considering the projected increase in manufacturing capacity under PO1, largely through brownfield expansions, calculations indicate that Scope 1 emissions would be around **0.064 tCO2e per wafer**, while Scope 2

emissions would account to approximately **0.325 tCO2e per wafer** on a location-based basis and **0.288 tCO2e per wafer** on a market-based basis([176]). These results are in line with the imec.netzero multi-parametric life-cycle assessment model of the environmental footprint for the fabrication of integrated circuits in a high-volume semiconductor fab – **0.08 tCO2e per wafer** for Scope 1 emissions and **0.42 tCO2e per wafer** for Scope 2 emissions.([177]) Water withdrawal is estimated to increase by about **10.75 m^3 per wafer**.

Under PO1, more favourable policy frameworks would lead to a manufacturing capacity growth rate of 4% from 2030 onwards. This would lead to a capacity of 20.3 million wafers per year, which in turn would account to between 1.3 – 1.6 Mt CO2 in Scope 1 emissions and 6.6 – 8.52 Mt CO2 in Scope 2 emissions (location-based). Overall, the environmental costs under PO1 are estimated to be between EUR 1.5 – EUR 2.4 billion (taking into consideration aggregated Scope 1 and 2 emissions (location-based)).

Accelerated permitting, clearer and more predictable regulatory frameworks, and improved infrastructure coordination can support earlier deployment of resource-efficient technologies and facilitate access to low-carbon and renewable energy. Targeted support for research, development and innovation under **PM1** is also expected to improve energy, water and material efficiency over time.

From a climate perspective, PO1 is broadly aligned with EU climate objectives, including the 2030 emissions reduction target and climate neutrality by 2050. The small increase in emissions per wafer, combined with Europe's low-carbon electricity mix and growing renewable capacity, limits the risk of a significant rise in absolute greenhouse gas emissions. Overall, the environmental and climate impacts of PO1 would be **incremental, manageable and compatible with decarbonisation pathways.**

6.1.3 Social impacts

6.1.3.1 Impact on skills.

PO1 through PM7 aims to rapidly address ongoing skills shortages, which in Europe is currently estimated at **100,000 engineers**([178]), **while establishing a robust talent pipeline for the semiconductor ecosystem.** This focus is supported by feedback from the open public consultation, **where 94% of respondents agreed that serious talent shortages** require investment in attraction, skilling, reskilling and training policies (with 65% strongly agreeing). This option would combine short-term interventions designed to mobilise available labour with long-term structural reforms to strengthen the EU's education and training capacities. It would respond directly to industry demands, labour market projections and Member State feedback gathered during the evaluation of the Chips Act.

([176]) All calculations are presented in Annex 4, section 4.
([177]) Die Setup - imec.netzero; technologies: N28 (Logic Mobile SoC, 300 mm), Germany - average ; 10 mm die size X and die size Y: yield 85%; IPCC Tier 2C with combustion abatement model.
([178]) McKinsey & Company. (2024). *McKinsey on semiconductors: Creating value, pursuing innovation, and optimizing operations* (No. 9, March 2024). McKinsey & Company.

Evidence points to a significant tightening of the talent pipeline: analysis referenced by the European Chips Skills Academy indicates that **around 30% of the current semiconductor workforce is expected to retire between 2023 and 2030**, increasing replacement and upskilling needs. In addition, an ECSA stakeholder survey identifies **chip design profiles as a critical shortage**, with **52% of firms** reporting them among the most sought-after roles. These constraints reinforce the rationale for PM7 as a prerequisite for scaling advanced manufacturing and the EU's fabless ecosystem.

PO1 would support **targeted upskilling and reskilling programmes** to support the rapid adaptation of the existing workforce. These programmes would enable engineers to transition from digital design to analogue and system design and equipment manufacturing workers with the competencies needed to operate AI- and robotics-based tools and manage associated data processes.

Figure 18 - EU regions facing a talent gap versus talent surplus in semiconductor industry (Source: European Skills Strategy 2025)

To ensure long-term resilience, PO1 foresees significant **expansion of training capacities in critical semiconductor fields**. Dedicated training hubs would be created for highly specialised profiles such as system designers, analogue designers and cybersecurity experts, where severe shortages are expected by 2030. In addition, the option targets reinforcement of electrical and electronic engineering programmes, with a particular focus on Member States where capacity is insufficient or declining. PO1 would promote the deployment of modern digital learning infrastructures, including virtual labs, simulation platforms and remote learning environments, to ensure high-quality training across the Union. Concrete implementation of these activities would rely on the Chips JU and its successor.

The lack of available design talent in the Union has contributed to firms expanding their design workforce in other regions rather than in the EU, underscoring the relevance of

targeted skills investments to retain and grow high-value activities in Europe.([179])**Therefore the successful delivery of skills measures under PO1 would rely on strong industrial participation**. Companies would be encouraged to support the development of curricula with universities and vocational providers, contribute to specialised short courses and training modules, and systematically engage in updating educational content according to technological evolution. **Furthermore, considering that skills are a national competence, the effectiveness of PM7 under PO1 also relies on the capacity of Member States and regions to absorb the increased resources.**

6.1.3.2 Impacts on territorial cohesion.

As stated by the European Semiconductor Regions Alliance (ESRA), the European semiconductor value chain **"**thrives on proximity**,** where co-located firms, research institutions, and supply chain partners create synergies that amplify innovation and production**"** ([180]). This points to how important the European semiconductor value chain can be as an engine for regional development and cohesion. PO1 introduces **under PM4 the Semiconductor Regions of Excellence label,** which would set voluntary standards for regions to support their local semiconductor industry and streamline compliance requirements.

This measure would recognise regions who have direct measures in place to support the semiconductor value chain in their region and aims to encourage additional regions to also take supportive measures. The increased reputation of a region, for its excellence in the semiconductor sector, through the **PM4** label, will improve the visibility of said regions as potential targets of investment into their local semiconductor ecosystem. A Network of European Semiconductor Regions of Excellence would be established to exchange best practices and encourage regions to develop complementary industrial strategies in synergy. In this way, **PO1**, especially under **PM4**, is expected to have positive impacts on cohesion and regional prosperity. The level of effectiveness of this measure will depend to a large extent on the reputational value the label acquires to compel regions to take the necessary steps to grow their semiconductor ecosystem.

6.1.3.3 Impacts on security of supply

PM2 would clarify the scope of FOAK to encompass the wider semiconductor value chain and to allow the financing of projects of public interest where these demonstrably contribute to **the EU's security of supply and economic security**, thereby addressing key vulnerabilities in the EU semiconductor supply chain as identified under **P1**. By strengthening support for identified supply chains, **PM2** would help safeguard the functioning of the Single Market and significantly enhance EU-level crisis preparedness and response, notably through improved availability of chips in crisis. **PM10** would incentivise the supply of semiconductor in critical infrastructures from domestic undertakings or from third countries which can guarantee security of supply. While the overall benefits cannot be fully quantified, they are

([179]) Final-Skills-Strategy-2025-Nov2025.pdf
([180]) ESRA, Home - European Semiconductor Regions Alliance

expected to generate a **substantially positive impact on security of supply** by ensuring continuity of essential goods and services during crises across the Union.

6.1.4 Governance

6.1.4.1 Impacts on governance

PO1 introduces a set of industry-driven transparency tools aimed at improving situational awareness and strengthening the Union's capacity to anticipate, detect and mitigate semiconductor supply chain disruptions, while minimising administrative burden and protecting business confidentiality **(PM6).** Under this option the Union would support the establishment of a **Business-to-Business Semiconductor Supply Chain Platform** (**PM5**) for companies across the semiconductor value chain building on the recommendations of the Working Group on Supply chains from the Industrial Alliance. ([181]) The Platform would operate as a **secure digital twin of the supply chain**, enabling participating firms to upload information, which would then be anonymised and aggregated. Companies would benefit from aggregated insights on supply chain risks, thus supporting internal resilience-building and **reducing their own market-information costs**. The platform would be managed by a trusted intermediary on a secure data-sharing infrastructure and in compliance with Article 101 TFEU. The Platform would mitigate part of these risks by **enabling trusted, privacy-preserving multiparty computation** and faster, more reliable information-sharing across the semiconductor supply chain. By providing earlier visibility on supply constraints, demand surges, and potential single points of failure, the Platform could reduce **downstream exposure to global shocks and limit the economic impact of disruptions**. The type of information shared through the Platform would be largely determined by participating industrial stakeholders and is expected to relate to key supply chain metrics, such as availability-to-promise (including available quantities and lead times). To ensure broad participation and compliance, the measure would be accompanied by supporting actions (i.e., technical assistance and interoperability standards) aimed at reducing implementation costs and facilitating effective uptake. The cost for the large companies is estimated at around EUR 100 000 for the initial year (including setting up the API connectors) and then EUR 50 000 for the yearly operations. ([182])

PM5 is expected to generate substantial economic benefits by reducing the severity and duration of potential supply chain disruptions. Public authorities and industry benefit from the Platform's real-time risk mapping, which enables faster crisis response and reduces downstream disruption costs. Evidence gained from the workshop on supply chains and the Call for Evidence ([183]) showed that **supply chain transparency infrastructure** should be considered a core priority. Participants called for establishing platforms that collect and share real-time information about disruptions, capacity, and supply levels whilst respecting commercial sensitivities.([184])

([181]) Working Group on Supply Chains | ALLPROS.eu
([182]) Annex 3 of the Impact assessment.
([183]) SEMI Europe Publishes 30 Recommendations for a Forward-Looking European Chips Act | SEMI
([184])Annex 2 Section 8

The caveat is that **quantifying the precise impact of such a measure is inherently difficult as geopolitical and security risks are the main factors.** For the purpose of this impact assessment, the analysis focuses on illustrating **what is economically at stake in the absence of improved coordination and early-warning mechanisms**. In 2023, two major consuming sectors of semiconductors - motor vehicles and transport equipment (EUR 934 billion) and machinery and equipment (EUR 600 billion) - generated over **EUR 1.53 trillion in production value.** ([185]) Without an EU-wide monitoring and crisis-anticipation mechanism, this output remains vulnerable to semiconductor supply shocks. In a **worst-case scenario** driven by major geopolitical disruptions, **more than EUR 1.5 trillion in annual economic activity in these sectors alone could be at risk** if alternative capabilities are not secured within one year.

Two examples from recent years provide additional observable evidence. During the 2021–2022 global semiconductor shortage, the European automotive industry incurred losses estimated at over EUR 100 billion. ([186]) While the semiconductor market is inherently cyclical, the structural vulnerabilities that contributed to this crisis persist and as described under **PD1**, have in some respects intensified due to the current geopolitical context. Industry data suggests, for example, that the chip shortfall linked to the Nexperia case could result in more than **EUR 5 billion in lost output** for the affected sector in the final quarter of 2025 alone. ([187])

Additionally, the option would further refine the Chips Act's information request on an ad-hoc basis, to assess potential pre-crisis stages with a view to identifying the appropriate and proportionate content of such a request **(PM6).** The requests would ensure that industrial stakeholders are not required to disclose business-confidential or commercially sensitive data. Instead of granular, company-specific datasets, the Commission could ask for **information request** - supported where possible by aggregated, non-sensitive data sourced from the Platform and if judged insufficient directly by companies. Such requests **would only be applicable under strict safeguards**. This soft approach reduces compliance burdens, ensures principles of proportionality, and enhances trust and cooperation between industry and public authorities. Burden per request for information can be estimated at **10 days/person and hence less than 0.1 additional FTEs. ([188])** This can be translated into EUR 2782 per request and hence negligible and appropriate, compared to the potential savings in anticipating a crisis. Transmission of these requests would take place through a secured communication and information could only be used for the purpose of this request.

The safeguards would be similar to the ones provided in the articles 25 and 32 of the Chips Act (which concern information gathering after the crisis stage is activated and treatment of confidential information respectively). The safeguards should remain flexible enough though to enable the Commission to request information. The requested information shall be limited to what is necessary: **to assess the nature of the potential semiconductor crisis and to identify and assess potential mitigation or emergency measures at Union or national**

([185]) https://ec.europa.eu/eurostat/web/products-eurostat-news/w/ddn-20240724-1
([186]) Missing chips cost EUR100bn to the European auto sector | Allianz
([187]) Europe's Carmakers Brace for Severe Chip Supply Crisis
([188]) Annex 3 of the Impact assessment.

level before a formal crisis activation (thus for preparedness of the Commission and Member States in case private sector preparedness measures are not enough and public intervention is required) or **to assess whether initiating the procedure referred to in Article 23 of the Chips Act (crisis activation) may be necessary and proportionate**.

These requests for information shall state the legal basis and purpose of the request, be limited to what is necessary and be proportionate in terms of volume of the data and frequency of access to the data requested, set out the time limit within which the information is to be provided and possible penalties for incorrect, incomplete or misleading information. This request for information should always be accompanied with a request to join the platform.

This approach ensures consistent data availability and harmonised monitoring practices across the Union. This targeted access to detailed datasets would allow the Commission to assess specific bottlenecks, dependencies or disruptions with high precision, before reaching the crisis activation stage, thereby improving the effectiveness of proactive crisis-avoidance or mitigation measures. Appropriate safeguards would be applied to ensure strict protection of business-confidential information, proportionality of requests, **and compliance with EU data protection and competition rules.**

The combined implementation of **PM5** and **PM6** would significantly strengthen the EU's ability to anticipate and mitigate semiconductor supply chain risks, particularly by improving **SO3** monitoring capabilities. This would enable a more agile, effective, and proactive response to potential crises.

6.2 PO2 "STRATEGIC SOVEREIGNTY"

PO2 includes several key measures: designating Strategic Projects in line with the proposed Competitiveness Fund to support initiatives under Pillar II, deploying innovation procurement and lab-to-fab accelerators, and strengthening the Union's capacity for crisis preparedness. **PO2** would also absorb all the policy measures under **PO1**.

6.2.1 Economic impacts

6.2.1.1 Impacts on EU semiconductor firms' revenues

6.2.1.1.1 Semiconductor firms

Strategic Projects (**PM8**) are expected to increase the revenues of EU semiconductor firms, with outcomes depending on the technological orientation of the investments. Assuming a potential public budget envelope of EUR 15 billion from the EU via the ECF and from Member States for the **sovereign manufacturing stream**, two scenarios can be considered. As set out in Annex 4 Section 5, if new capacity broadly follows the current European wafer mix, which is dominated by mature and specialty nodes, this investment would approximately generate **up to EUR 6.6 billion** in additional annual revenue. In an alternate scenario where part of the investment supports a leading-edge logic fab while the remainder follows the existing mix, the higher value added would result in a significantly larger market impact of **up to EUR 11.5 billion per year**. Together, these scenarios provide lower- and upper-bound estimates of the revenue effects of Strategic Projects, depending on whether investment reinforces the current industrial structure or enables a partial shift towards advanced manufacturing. For simplicity of analysis, this projection considers only front-end

manufacturing since quantifying revenues from back-end facilities is more complex due to the heterogeneous nature of back-end facilities, which are discussed further in Annex 4 Section 5.

Under the **chip design stream** of **PM8**, the Union and Member States, through their support of designs of strategic importance to the Union such as those for AI chips, are expected to have a net positive impact on the revenues of European semiconductor firms. Public support is likely to de-risk early-stage design activities, accelerate time to market, and enable firms to address high-growth segments with strong global demand. This, in turn, would for example support higher licensing income, increased sales of proprietary designs, or gain in market share for EU-based fabless companies. By strengthening the Union's presence in advanced and application-specific chip design, notably for AI and high-performance computing, these measures are expected to contribute to higher value added and more resilient revenue streams, compared to a continuation of current market trends without targeted public intervention. Because the chips design stream could potentially support a wide variety of designs, end uses, and technology combinations, with heterogeneous business models and revenue channels, it is difficult to quantify its aggregate impact on semiconductor firms' revenues in a robust manner.

The implementation of grand challenges under **PM9** would substantially boost revenues for EU fabless SMEs by leveraging innovation procurement to provide early demand, enable reference deployment and accelerate market entry for leading-edge designs. It would reduce upfront capital constraints and shorten time-to-market, allowing SMEs to reach commercialisation milestones faster and demonstrate market readiness to attract private investors and further sales orders. By formulating mission-oriented requirements in key strategic areas (cloud, automotive, edge, robotics), these challenges would foster differentiated European IP and application-specific chips, enabling SMEs to capture market share in high-growth segments.

Furthermore, as explained in Annex 6, the use of innovation procurement (**PM9**) would enable SMEs to validate technologies early on, making them more attractive for venture capital and investment.

Through support for **lab-to-fab accelerators (PM9),** semiconductor firms are expected to benefit from faster translation of research results from Europe's world class research institutes into commercially viable products thus reducing development timelines and associated costs. By lowering technological and financial barriers, these measures would enable firms to bring new designs and process innovations to market more quickly, improving their ability to capture early revenues in fast-moving segments.

Together, **PM8** and **PM9** will significantly contribute to achieving SO1 and SO2. By 2035, they will contribute to enable the creation of 200 EU-incorporated semiconductor value-chain start-ups (spinouts or new ventures) that reach at least a seed funding round. Additionally, by 2035, PM9 will contribute to grow the EU's indigenous demand for European solutions by securing EUR 5 billion in innovation procurement for semiconductor-enabled solutions across the automotive, industrial, energy, AI, health, and telecoms sectors, and will deliver at least one flagship co-development project per sector.

6.2.1.1.2 Value chain

Under the value chain stream of Strategic Projects (**PM8)**, the Union would have the means to co-invest with Member States in industrial support for companies across the semiconductor value chain, thereby strengthening revenue generation beyond a single segment (for example, manufacturing) and supporting more balanced growth across upstream and downstream activities.

The value-chain wide and cross-border nature of Strategic Projects would **strengthen cluster dynamics, reduce fragmentation and enable progress in segments that require coordinated progress across several stages of development**. Such investments would de-risk investment in the value chain and thereby encourage European firms to develop new capabilities or build competitive advantages that would enable increases in market share and increased revenues. They would contribute to better integrate SMEs and SMCs into the European semiconductor ecosystem with the potential to increase the value chain's resilience by for instance providing innovative solutions or alternatives to current dependencies.

6.2.1.2 Impacts on manufacturing capacity

PO2 marks a step change from the BAU scenario and PO1, where support from the Union's budget is focused on classical R&I support under the research framework programme. Under PO2, through **PM8**, assuming a EUR 15 billion public investment for front-end manufacturing that in turn generates an additional EUR 25 billion in private investment, in line with aid intensities seen in previous FOAK cases, it is estimated that investment through **PM8** would generate, if coupled by improved framework conditions, around **222,000 additional wafers per month** if projects broadly follow the current European wafer mix and up to **108,000 wafers per month** if the investments would include a leading edge facility.

Since budgets are not yet defined and therefore concrete impact analyses are difficult, an assessment was undertaken to illustrate the potential scale of outcomes from Strategic Projects, based on a total investment envelope of EUR 40 billion (public and private combined).

In the analysis of impacts, two scenarios were considered: either all projects would follow the profile of previous FOAK; or the project mix would include one leading-edge front-end manufacturing facility (Scenario 2), with the rest following the profile of previous FOAK projects.

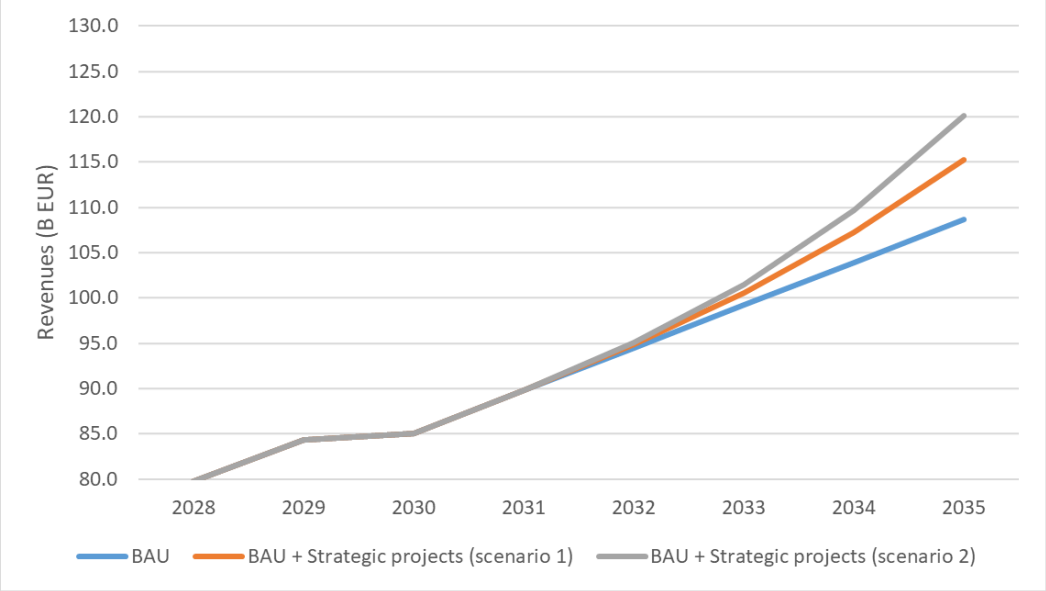

Figure 19 – Projected revenues generated through Strategic projects

Assuming this level of investment, funding for Strategic Projects would increase EU semiconductor manufacturing capacity within the range of ~108,000 to ~222,000 wafers per month, depending on the technology mix. Expansion following the current profile of the Union's manufacturing capacity yields higher volume, but lower value added (≈ EUR 6.6 billion additional annual revenue), while partial reallocation towards leading-edge manufacturing delivers lower capacity expansion but higher revenues (≈ EUR 11.5 billion per year). Outcomes reflect a trade-off between volume-driven growth and higher-value advanced-node production.

As set out in Annex 4, by analysing previous examples in the previous FOAK projects, a EUR 40 billion investment facilitated by Strategic Projects would generate 7301 direct jobs and 16,000-36,500 indirect jobs.

The lower wafer count under the second scenario is explained by the fact that a leading-edge facility would absorb more of the budget. However, this scenario would give Europe the sovereign means to manufacture leading-edge chips, crucial for AI systems amongst other applications.

Under the 'sovereign manufacturing' stream of **PM8**, support for back-end facilities is also foreseen to address vulnerabilities discussed in **PD2**, however forecasting manufacturing capacity in advanced packaging is less straightforward than for front-end fabs because output cannot be expressed in a single, comparable "wafers per month" metric. Packaging throughput depends on heterogeneous product mixes and process routes (for example, 2.5D/3D integration, fan-out, interposers, chiplets), with capacity constrained by different tools and steps and measured in units such as packages, substrates or panels rather than wafers. As a result, nominal tool capacity is highly sensitive to design choices (die size, layer counts, bump pitch, yields and test requirements), making forward-looking capacity estimates less comparable and less predictable than in front-end manufacturing. Furthermore, support under the '**supply chain resilience**' stream of **PM8** would enable the scaling up of manufacturing across the value chain from materials to equipment to design tools.

6.2.1.3 Impacts on demand

The envisaged capacity would be unsustainable without sufficient commensurate demand. As explained in previous chapters, the EU's demand for AI chips in data centre infrastructure and at the edge is expected to rise as AI continues to be deployed across industry and society([189]). The upcoming AI Gigafactories, the expected rise in data centre capacity through the upcoming Cloud and AI Development Act coupled with advances in robotics including humanoids but also, autonomous cars, other autonomous defence systems such as drones, immersive-reality technologies (wearables, smart glasses) and the broader AI-driven transformation of all sectors of the European economy create a great opportunity for the Union to channel this rising demand into the emergence of a new generation of fabless companies ([190]).

However, as set out in **PD3**, many start-ups face a critical gap beyond access to venture capital: the absence of potential anchor customers who can provide early revenue and help establish the credibility of their products. In addition, stakeholders during public consultation repeatedly expressed support for the introduction of demand-aggregation frameworks, enabling coordinated procurement across high-impact sectors such as defence, telecommunications, automotive, health and space. It is for this reason, that **PO2** incorporates a measure **(PM9)** related to **innovation procurement**. Such measure would allow start-ups and SMEs to be involved in projects involving not only the classical support for R&D but also eventual procurement by both public and private sectors, with this procurement being derisked by the Union's investment. This will mark a departure from the BAU approach where support is usually reserved for R&D grants. Innovation procurement is also a useful mechanism for the implementation of thematic grand challenges for leading-edge chip designs in different application areas such as datacentre AI accelerators, automated driving processors, edge AI solutions or AI processors for AI Factories and Gigafactories. Over time, more predictable demand would also help anchor ecosystem actors such as specialised materials suppliers and design houses within the EU market, contributing to broader market growth and contribute to the alleviation of **PD2**.

Empirical evidence([191]) indicates that competitive public procurement contracts for innovation can generate **persistent revenue effects (up to EUR 0.5 per euro of contract value)** and **crowd in private investment (around EUR 0.2 per euro of public demand)** over the medium term. Public procurement is also associated with **measurable reductions in firm-level risk and uncertainty**, particularly during periods of financial stress, supporting investment and resilience in capital-intensive sectors.

The intervention to incentivise chips from domestic or domestic-equivalent undertakings in public procurement of critical infrastructures (**PM10**) is implemented through a limited adjustment to existing procurement conditions and does not create new regulatory bodies or

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([189]) Decision based on Eurostat and WSTS.
([190]) McKinsey Technology Trends Outlook 2025 | McKinsey
([191]) Budrys, Z. (2025). *Consumer of last resort: Government procurement, firm-level evidence and the macroeconomy* (Working Paper). Retrieved from https://zymantasbudrys.com/wp-content/uploads/2022/10/ZymantasBudrys_JMP_LastConsumer.pdf. Refer to Annex 4, section 6 for more details.

compliance systems. Furthermore, contracting authorities already routinely specify security- and certification-related requirements for chips. Requesting a semiconductor supply chain declaration will remain optional, but recommended, for procurement authorities, which may take security of supply considerations into account when designing the technical specification and contract clauses, and consider the information provided in the declaration as criterion other than price when awarding the contract. Potential unit-cost effects are expected to be limited, as semiconductors for critical applications are often already provided by domestic undertakings and semiconductors represent a minor cost component within overall ICT procurement, except for data centres, for which domestic or equivalent undertakings already currently supply the near totality of the chips for the EU market. As a result, the measure is not expected to significantly increase public procurement expenditure while safeguarding security of supply for public infrastructures.

Estimating the policy-relevant market requires mapping semiconductor consumption across NIS2-defined sectors and applying a public procurement share to the resulting totals. The total **EU semiconductor consumption in NIS2-relevant sectors is estimated at approximately EUR 25.6 billion in 2025**, spanning industrial electronics including energy and water (EUR 5.4bn), digital infrastructure including telecoms and servers (EUR 14.9bn), automotive limited to NIS2-relevant applications (EUR 3.6bn), security and safety systems (EUR 1.2bn), health (EUR 1.0bn), defence (EUR 0.4bn) and aerospace (EUR 0.3bn).[192] Applying a public procurement share of 15 to 30%, consistent with OECD estimates for comparable economies[193], yields a chip value in publicly-procured NIS2 equipment of between approximately EUR 3.8 billion and EUR 7.7 billion.

Currently, undertakings which are neither domestic nor equivalent have a limited market presence in the semiconductor categories most relevant to NIS2 sectors, though the picture varies by product type. In the mature-node segments that dominate industrial, energy and automotive applications (analogue components, discrete semiconductors and microcontrollers) non-domestic suppliers have not yet captured significant EU market share. In industrial and energy procurement, the leading suppliers of analogue and power semiconductors remain predominantly European and North American, with Chinese competitors such as Hangzhou Silan and BYD Semiconductor together holding low single-digit market shares. In automotive and telecoms infrastructure, no non-domestic firm currently features among the top five suppliers by revenue in the relevant product categories.[194]

The data centre and AI segment, despite representing the highest chip values, carries the lowest exposure to suppliers who are neither domestic nor equivalent (signatories of agreements which would apply to the supply of semiconductor). Advanced-node components (AI accelerators and high-bandwidth memory) are exclusively designed by US companies and front-end manufacturing is concentrated in Taiwan and South Korea.

[192] Data by Decision Etudes & Conseil, forthcoming, 2026.
[193] Government at a Glance 2025 | OECD
[194] Q4 2025 Results | Infineon Technologies.

The most extreme hypothetical scenario, in which public procurement authorities in all sectors would choose to apply the most restrictive criteria on non-domestic semiconductor suppliers, would be a de-facto ban of non-domestic semiconductors. This would have the most significant practical effect on industrial, energy and transport sectors, where mature-node off-the-shelf components represent a potential area of growing exposure as non-domestic suppliers seek to gain market share through artificially low pricing. Even in these sectors, however, switching costs rather than unit price differentials are the primary concern: replacing components typically requires extended qualification timelines, design adaptation and in some cases recertification, meaning that the measure's effects would materialise primarily over a medium- to long-term horizon.[195] Exception clauses for cases of unavailability, disproportionate cost or technical incompatibility are therefore operationally essential, particularly in the short term, and would need to be applied with sufficient precision to avoid supply disruptions in time-sensitive procurement contexts.

The **self-declaration mechanism** places most of the compliance burden on tenderers, who are best placed to map their own supply chains, rather than on contracting authorities, who typically lack the commercial data or technical expertise to verify chip provenance independently. This approach avoids the creation of new regulatory bodies or product-level approval procedures and is administratively lighter than a pre-certification regime. However, self-declaration alone does not eliminate the need for oversight: competent authorities would still need to audit a proportion of declarations and verify the credibility of supplier origin claims, requiring dedicated technical capacity at EU or Member State level.

Tenderers may sometimes be several steps removed from the original chip vendor, as OEMs frequently do not track chip-level provenance through their supply chains, and for commodity or off-the-shelf components, the specific chip models and their geographic origin may not be commercially disclosed (one aspect that the proposed measure is expected to change).[196] They would need to bear some costs, which however would have to be weighed against the costs of increasingly-likely supply chain disruptions due to poor visibility of dependencies, as happened during the COVID-19 pandemic or with the Nexperia case.

6.2.1.4 The cost (price) competitiveness of the EU industry

As under **PO1**, the EU is expected to remain at the higher end of the global cost curve for semiconductor manufacturing, reflecting structural factors such as comparatively higher energy and labour costs (as set out in PD2). However, **PO2** would further reduce investment and operational risks through a combination of Strategic Projects (**PM8**) and demand-side initiatives (**PM9, PM10**) alongside continued support via First-of-a-Kind (FOAK) projects, complemented by enhanced supply chain transparency and the framework conditions improvements already present under **PO1**. On capital costs, **PO2** is expected to improve investment feasibility beyond **PO1**. Under **PO1**, faster permitting, coordinated infrastructure planning and clearer regulatory processes would continue to reduce delays and associated financing costs relative to BAU. Under **PO2**, these effects would be emboldened through EU-level co-funding for Strategic Projects (**PM8**), which would lower upfront capital

[195] Vulnerabilities in the semiconductor supply chain | OECD
[196] Comments of the Semiconductor Industry Association on the NIST Internal Report NIST IR 8536 2pd | SIA

requirements for selected large-scale investments and reduce the cost of capital by lowering risk premia. This would partially mitigate the EU's structural cost disadvantage described in **PD2**.

Demand-side measures such as innovation procurement (**PM9**) and incentivised procurement from domestic or equivalent undertakings (**PM10)** are expected to support capacity utilisation by strengthening downstream demand and supporting the scaling-up of European fabless and system firms. Higher utilisation rates, by a scaled-up European fabless ecosystem, would support lower unit costs for foundries by spreading fixed costs over a larger output base and reducing the effective capital expenditure per unit of output relative to BAU. While construction and equipment costs would remain broadly unchanged, lower financial risk and reduced underutilisation risk would improve the realised cost position of supported facilities. Supply chain transparency (**PM6**) would not materially reduce OPEX, though better visibility of critical inputs could enable the Union to proactively address issues and reduce unplanned stoppages and operational volatility. This could support improved cost predictability, with indirect positive effects on competitiveness through reduced downtime.

When it comes to price competitiveness, as further elaborated on in Annex 5, PO2 would strengthen the EU's position in specialised higher-value segments where reliability, co-design and advanced packaging are critical differentiators, all elements that could be supported by **PM8.** While global cost hierarchies would still reflect structural factors such as energy prices and ecosystem density, **PO2** would meaningfully enhance the EU's competitiveness and enable diversification beyond current markets and strengths into future, high-growth markets. Strategic Projects could support specialised nodes or packaging technologies with higher value per wafer, improving pricing flexibility relative to BAU.

6.2.1.5 Impacts on public budgets

This subsection assesses how **PO2** would affect public budgets relative to the baseline, covering EU and national expenditure and administrative costs. Under BAU, significant resources are already committed to the semiconductor ecosystem with approximately EUR 43 billion in combined EU and national support for 2023-2030. **PO2** would go beyond this baseline by introducing EU-funded (and Member States co-funded) Strategic Projects (**PM8**), demand-side tools (**PM9, PM10**) and mandatory information mechanisms for qualitative data, resulting in **higher and more concentrated public expenditure,** including administrative costs, than under either **BAU** or **PO1**.

At EU level, the largest fiscal effect would come from the creation and co-financing of Strategic Projects (**PM8**). Unlike **PO1**, which increases R&D&I support but does not fund manufacturing investments, PO2 requires substantial EU contributions for cross-border projects in sovereign manufacturing, advanced packaging, design and supply chain resilience. These allocations would represent a significant deviation from the baseline in both scale and intensity, covering capital investment and multi-year coordination. Demand-side measures, such as innovation procurement, would also require EU resources beyond **BAU** and **PO1**, dependant on procurement volumes.

Union budget depends on the outcome of the next MFF discussions. However, EU level support, the main source of funding would come from the proposed ECF, should it materialise. On the national side, possible sources of financing include cohesion funds.

Under **PM8**, a public-private investment in the range of **EUR 40 billion** would ensure a sufficiently robust investment package on front-end manufacturing to address the leading-edge manufacturing vulnerability thus protecting the Union from geopolitical dependencies or economic coercion as set out in **PD1** while also having further room for investment in front-end facilities in line with Europe's demand profile that continue building on the ongoing FOAK investments.([197]) Recent State aid intensities for FOAK projects in Europe, aid is usually at around 30-40% of the project's total costs. This would imply a public investment (EU and Member States) of **EUR 15 billion**.([198])

PM8 would also cover back-end investment in advanced packaging and testing, especially 2.5D/3D integration and chiplet-based architectures. These capabilities are increasingly decisive for performance and time-to-market in AI/HPC, automotive and other applications, and would reduce critical EU overdependencies on third-country packaging capacity.

Considering the fact that the Union will for the first time be deploying direct management funding via the ECF for manufacturing capacity, additional administrative resources will be necessary. As set out in Annex 3, around **12 FTEs** would be required to supervise and administer Strategic Projects.

Further measures would be necessary to support design and the broader value chain, although considering the heterogeneous nature of such activities, it is difficult to quantify such support in generic terms. A notable example would be support for strategic design assets (including IP blocks) in the area of AI chips. Here, for leading edge technologies budgets can be significant. In fact, the cost of development of an advanced design at a 2nm technology node may reach up to USD 1 billion,([199]) with public support under Strategic Projects supporting a portion of this figure.

In PO2, national budgets would be supported by the EU budget via the ECF when compared with BAU and with **PO1**. Strategic Projects require coordinated co-funding by EU, national and industry partners, implying that participating Member States' budgets would face lower budgetary pressure than when compared to granting State aid alone. Furthermore, this expenditure could generate fiscal returns such as higher long-term tax revenues.

Furthermore, successfully scaled Strategic Projects may generate fiscal returns through personal income taxes and social contributions from direct and indirect employment, as well as corporate taxation linked to additional semiconductor revenues. Based on estimated employment effects (direct and indirect), and additionally generated revenues, the initiative is expected to yield positive net fiscal flows over time, partially offsetting public support. Based on the modelling presented in Annex 4 in Section 5 Strategic Projects might imply annual direct fiscal returns of between EUR 380 million and EUR 662 million.

([197]) Further discussed in Annex 4.
([198]) All listed budgets are for illustrative purposes only and are without prejudice to the negotiations of the upcoming Multiannual Financial Framework for 2028-2035.
([199]) IBS, Global Semiconductor Industry Service, Analysis of Design Costs, September 2024.

6.2.1.6 Impacts on R&D and innovation ecosystem

Semiconductor R&D and innovation would benefit substantially from **PO2**. Strategic Projects under the proposed ECF will be enabling the industrialisation of a greater share of research from publicly funded programmes, including from the pilot lines under Pillar I. Given that much of the innovation in the semiconductor industry involves process optimisation and requires close interaction between laboratory work and manufacturing environments, the expansion of production activities in the EU supported by the Chips Act could also stimulate additional R&D through the need to co-locate research with fabrication. A potential bottleneck, however, is the shortage of skilled scientists and engineers, especially when moving to below 2nm nodes, a challenge already well-documented in the European semiconductor sector.

Furthermore, greater public backing may encourage firms to commit more of their own resources to higher-risk R&D projects, knowing that stronger public support reduces the financial uncertainty associated with such efforts. In addition, empirical evidence suggests that participation in innovation-oriented public procurement is associated with 10–20 percentage point higher probabilities of product innovation, and around 6 percentage point higher probabilities of process innovation, compared to otherwise similar firms ([200]), ([201]) (see Annex 4, section 6 for more details).

6.2.1.7 Impacts on SME/start-up ecosystem

Start-ups and SMEs would also benefit significantly from **PO2**. The semiconductor industry relies on a wide network of highly specialised smaller firms across the value chain, and increased investment through Strategic Projects under the ECF, together with an expanded scope for First-of-a-Kind projects, would stimulate additional demand for these specialised inputs.

Chip design is another area where start-ups and SMEs stand to gain especially since the EU's fabless companies are almost entirely SMEs whose work is within scope under Strategic Projects (**PM8**).

Furthermore, through the deployment of innovation procurement, start-ups and SMEs can benefit from anchor customers that grant them the first revenues while also serving as a testbed for validation of technology and a pull-factor for further investment. Therefore, beyond firm-level revenues, innovation procurement under **PM9** would strengthen the SME/start-up ecosystem through innovation-to-market routes with clear technical milestones, testing environments and first deployments. By providing reference projects, access to testbed and integration partners, this approach reduces market-entry risks and information asymmetries for investors and customers, improving SME's ability to raise follow-on

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([200]) Andrea Bastianin, Paolo Castelnovo, Lorenzo Zirulia, Overcoming the innovation threshold through innovative public procurement: evidence from CERN, *Industrial and Corporate Change*, Volume 34, Issue 5, October 2025, Pages 871–900, https://doi.org/10.1093/icc/dtaf004

([201]) Dragana Radicic, Effectiveness of public procurement of innovation versus supply-side innovation measures in manufacturing and service sectors, *Science and Public Policy*, Volume 46, Issue 5, October 2019, Pages 732–746, https://doi.org/10.1093/scipol/scz026.

financing and scale internationally while stimulating cluster effects across the full hardware/software stack and across the European semiconductor value chain.

Design-focused SMEs could also benefit from new investments in advanced chip fabs. Such facilities would shorten and accelerate innovation cycles by reducing reliance on long third-country supply chains and exposure to fluctuating lead times, enhance customer trust when handling sensitive technologies, and offer manufacturing opportunities for lot sizes that large global fabs may consider too small or too specialised.([202])This support would complement existing BAU measures such as the Design Platform, pilot lines, Competence Centres and an expanded Chips Fund, all measures currently in place under the Chips Act. Taken together, increased technological support, improved framework conditions including financing, and the emergence of new manufacturing capacities could be transformative for design-oriented SMEs and start-ups, providing accessibility, speed, security, specialisation and ecosystem benefits that are difficult to obtain from traditional global players.

6.2.2 Environmental impact

When it comes to environmental impact, two scenarios are considered in Section 4 of Annex 4. In **scenario 1**, ([203]) the additional capacity generated by PM8 through EUR 15 billion in public investment would reach around 1.8 Mio wafers per month, leading to around 22.0 Mio wafers per year overall capacity. This expansion would be associated with estimated total scope 1 emissions of 1.4 - 1.7 MtCO2e and scope 2 emissions of 7.1 - 9.2 MtCO2e on a location-based basis, and water withdrawal of around 236.5 Mio m^3 per year([204]). Total water withdrawal represents an 8.5% increase compared with the baseline; a magnitude comparable to mainstream capacity expansions outside Europe. **Scenario 2** combines the expansion of mainstream nodes with the establishment of one leading-edge fab.

New mainstream capacity would amount to the addition of around 997,596 wafers per year resulting in a total capacity of around 20.4 Mio wafers per year, with estimated total scope 1 emissions of 1.3 – 1.6 MtCO2e, scope 2 emissions of 6.6 - 8.5 MtCO2e on a location-based basis, and water withdrawal of about 222.5 Mio m^3 per year. The leading-edge fab, modelled on industry data and assumed to reach 300 000 wafers per year, would generate around 74 555 – 79 005 tCO2e for scope 1 and 290 740 - 310 509 tCO2e for scope 2 on a location-base basis (assuming average annual increase of 5.79% in emissions per wafer due to rising process complexity). All details of the calculation are provided in Annex 4 - section 4.

Overall, scenario 2 would result in total emissions of about 1.4 - 1.7 MtCO2e for scope 1, 6.9 - 8.8 MtCO2e for scope 2 on a location-based basis with a total water withdrawal of approximately 222.3 - Mio m^3 per year. While European fabs currently recycle around 10–14% of water, non-European fabs in water-scarce regions such as Taiwan achieve reuse rates of about 80%, indicating significant potential for Europe to improve efficiency and competitiveness through advanced water management. In parallel, the shift to leading-edge

([202]) A methodological toolbox to monitor the semiconductors' supply-chain, Publications Office of the European Union, Luxembourg, 2024, doi:10.2760/5085463, JRC138921.
([203]) Projects following the technology mix typical for European firms.
([204]) All calculations are presented in Annex 4.

nodes and advanced packaging would increase material use, as mask layers rise from around 40 at 65 nm to up to 110 at 5-3 nm and additional packaging steps are required. As a result, Europe's total material consumption could increase by up to 65%, broadly in line with trends already observed in leading non-European semiconductor manufacturing hubs.

6.2.3 Social Impacts

6.2.3.1 Impacts on the labour market

Strategic projects and demand-side measures in PO2 will lead to considerable positive effects on jobs in the European semiconductor industry. These effects will be even larger when employment effects during construction of new fabs and further up the supply chain are also considered. A modelling of potential employment impacts shows that due to the Strategic Projects alone, if EUR 15 billion in public funding is dedicated to sovereign manufacturing, one should expect between **4,700 and 7,300 new direct jobs** ([205]) and an additional **16,000** to **36,000** indirect jobs (depending on other external factors, but projected with a good degree of confidence from the current first-of-a-kind investment). Direct jobs in the semiconductor industry are also reported as high-quality, as reflected in above-average salaries.([206]) Stronger support for design activities in start-ups and SMEs will also add to employment growth, since these are currently more labour-intensive than automated semiconductor production.

6.2.3.2 Impacts on territorial cohesion

The European semiconductor value chain ***"thrives on proximity, where co-located firms, research institutions, and supply chain partners create synergies that amplify innovation and production"*** ([207]), which makes the fostering of regional semiconductor ecosystems a powerful engine for regional growth and cohesion. PM8 aims to deliver investments across the European semiconductor value chain. From a cohesion policy perspective, this can lead to spillover effects and multiplication of investment across regions that may not be directly involved in the semiconductor value chain, but in its upstream markets.

PO2 is therefore expected to deliver significant benefits for cohesion and regional prosperity, with the additional funding serving as an incentive for regions to adopt enabling measures and invest in the development of their semiconductor ecosystems.

6.2.3.3 Impacts on security of supply

The availability of EU-level co-funding under PO2 would **enable the Union to invest in facilities that would serve the common European interest by ensuring the availability of critical manufacturing capacity, particularly when it comes to leading-edge chips,** where

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([205]) See Annex 4.
([206]) For example, in the US case, according to the White House Council of Economic Advisers, the median annual wage in semiconductor and other electronic component manufacturing exceeds that in overall manufacturing and is nearly double the median for retail trade jobshttps://bidenwhitehouse.archives.gov/cea/written-materials/2024/03/20/u-s-semiconductor-jobs-are-making-a-comeback/
([207]) ESRA, Home - European Semiconductor Regions Alliance.

the Union has critical dependencies on third countries as discussed in **P1**. Furthermore, **PO2** would also enable greater integration and depth across the semiconductor value chain than the baseline. A Strategic Project could potentially involve several stages of the value chain, including design, manufacturing, advanced packaging and resilience-related activities. This structure would instil a cross-border dimension across Member States and encourage tighter collaboration between manufacturers, design firms, equipment suppliers and materials producers.

7 HOW DO THE OPTIONS COMPARE?

This chapter provides **a comparison of policy options** against the criteria of effectiveness, efficiency, and coherence as well as the principles of proportionality and subsidiarity.

7.1 Effectiveness

SO1: Under the baseline scenario, capacity expansion would continue to rely primarily on market-driven investment decisions within the existing framework. While some incremental growth is expected in areas where the EU already holds structural strengths, persistent bottlenecks related to investment risk, feasibility constraints and limited coordination are likely to constrain expansion in more capital-intensive and technologically advanced segments. As a result, the baseline scenario would only partially contribute to enhancing security of supply and would not materially address strategic gaps in advanced manufacturing and packaging. Persistent issues related to permitting duration, regulatory uncertainty and skills availability would continue to affect investment decisions and project execution, resulting in a suboptimal investment environment

Policy Option 1 would improve conditions for capacity expansion by addressing non-financial barriers, notably through faster and more predictable permitting, clearer regulatory requirements and a clarified framework for First-of-a-Kind facilities. These measures are expected to facilitate investment execution and reduce uncertainty. However, in the absence of targeted Union-level support or demand-oriented instruments, capacity expansion would likely remain concentrated in segments where the EU is already competitive, with limited impact on underrepresented technologies such as advanced logic or packaging. Additionally, Policy Option 1 focuses on horizontal framework improvements, including faster permitting, regulatory clarity and targeted skills measures. These actions are expected to ease long-standing non-financial barriers, improve predictability and support more reliable project implementation across the value chain.

Policy Option 2 builds on these horizontal measures while adding Union-level coordination through Strategic Projects. This additional layer aims to address feasibility constraints for large and technologically critical investments and promote deeper integration across design, manufacturing and advanced packaging. Policy Option 2 combines framework improvements with Strategic Projects and demand-side instruments. These measures would address feasibility constraints for large-scale and technologically critical investments by reducing investment risk and supporting earlier and more predictable utilisation of new facilities. This approach is expected to enable capacity development in both mainstream and advanced segments, including those relevant for sensitive and security-critical applications.

SO2: Under the baseline scenario, user industries would continue to face supply uncertainty and limited incentives to source semiconductors produced in the EU. Here, adoption of new semiconductor and AI-related technologies would largely depend on global market conditions and external suppliers, with limited impact on demand formation within the Union.

Policy Option 1 may contribute indirectly to demand development by improving supply stability and investment conditions, which could encourage adoption over time. However, it does not include instruments specifically designed to stimulate demand or provide offtake opportunities for new technologies. Policy Option 2 introduces demand-side mechanisms, notably innovation procurement, which would provide earlier and more predictable offtake for semiconductor and AI-related products. These measures are expected to facilitate faster adoption by user industries and strengthen linkages between EU-based production and downstream demand.

SO3: Under the baseline, monitoring and crisis preparedness would remain fragmented and largely reactive, limiting the Union's ability to identify vulnerabilities and anticipate disruptions.

Policy Option 1 would improve coordination and information exchange but would not fundamentally alter the scope or depth of monitoring capabilities. Policy Option 2 strengthens information requirements and establishes a Business-to-Business Semiconductor Supply Chain Platform, enabling more systematic and timely insights into vulnerabilities across the value chain. This would support earlier identification of risks and more proactive EU-level preparedness.

7.2 Efficiency

The baseline scenario entails no additional administrative, compliance or budgetary costs. However, it is the least efficient option, as it leaves major structural inefficiencies unresolved and allows substantial implicit economic costs to persist. Evidence from the evaluation and problem analysis shows that under the baseline, lengthy permitting procedures generate significant delay-related costs. Semiconductor projects in the EU face permitting timelines that are on average 7-8 months longer than in leading Asian jurisdictions, corresponding to cost penalties of around 3% of total project value (approximately EUR 600-650 million for a EUR 20 billion fab). In addition, limited monitoring and preparedness lead to reactive rather than proactive crisis management and large downstream losses. Recent shortages resulted in tens of billions of euros in lost output, including EUR 5 billion in the automotive sector linked to the Nexperia disruption and EUR 50-100 billion economy-wide losses reported during 2021–2022. While avoiding direct compliance costs, the baseline therefore performs poorly in efficiency terms.

Policy Option 1 improves efficiency by addressing process inefficiencies and coordination failures primarily through horizontal framework measures. Incremental costs relative to the baseline are limited. Additional administrative and compliance costs for industry are modest and mainly linked to coordination and information exchange; no continuous reporting or new operational requirements are introduced. Based on comparable EU frameworks and observed administrative burdens in similar regulatory settings, these costs correspond to low single-digit person-days per year for large firms. Costs for Member States and EU authorities relate mainly to enhanced coordination and limited monitoring capacity and are largely absorbed

within existing structures. Policy Option 1 does not introduce additional operational costs (such as energy or resource use), as it does not mandate new production capacity, new equipment or changes in production processes beyond firms' existing investment decisions. Against these limited costs, PO1 delivers noticeable efficiency gains by shortening permitting timelines, increasing regulatory predictability and reducing investment risk and delay-related costs.

Policy Option 2 builds on PO1 by introducing Strategic Projects, demand-side instruments and enhanced pre-crisis intelligence, resulting in higher incremental costs, but also more ambitious outcomes. Incremental costs include costs for industry, concentrated on firms voluntarily participating in Strategic Projects, notably through capital co-investment. Administrative and reporting costs linked to enhanced monitoring remain limited and proportionate: reporting is triggered only on an as-needed basis in pre-crisis situations, with preliminary estimates indicating up to 10 person-days per reporting cycle for large firms, and no continuous monitoring obligation. Public costs for Member States arise from co-financing Strategic Projects and strengthened administrative capacity. Under PO2, additional operational costs (including energy and resource use) arise only from voluntary capacity expansion under Strategic Projects and are inherent to increased production rather than to regulatory compliance obligations. These costs are directly linked to measurable benefits. Strategic Projects are expected to generate EUR 6.6-11.5 billion in additional annual revenues, while EU co-funding reduces investment risk, lowers the cost of capital and enables earlier and more predictable utilisation of new capacity. Enhanced intelligence reduces the probability and severity of supply disruptions, mitigating losses that have previously reached tens of billions of euros.

Overall, PO2 can be considered efficient. While it entails higher costs and implementation risks than PO1, these are proportionate with the scale of the economic security risks addressed. The cost of inaction would leave the Union exposed to persistent vulnerabilities and potentially very large disruption-related losses that would significantly exceed the incremental costs of the intervention.

While Policy Option 1 achieves efficiency gains through a low-cost, proportionate intervention with limited administrative and compliance burdens, and Policy Option 2 entails higher incremental costs and implementation complexity, the latter also delivers higher expected benefits in terms of avoided disruption losses, risk reduction and revenue generation; as a result, both options can be considered to achieve a comparable level of efficiency when assessed as the ratio between costs incurred and results achieved.

7.3 Coherence

Internal coherence. All options are internally coherent, as they build on the three-pillar structure of the Chips Act, providing a consistent intervention logic that address a multitude of policy areas from R&I to manufacturing and crisis preparedness under a common governance framework. The scope of Chips Act 2.0 is unchanged across options.

Coherence with EU policies and legal frameworks. The baseline remains formally coherent with existing EU policies and internal market, competition and State aid rules, as it essentially maintains the current framework. However, it makes limited use of complementarities with newer priorities on competitiveness, economic security and strategic technologies. Policy

Option 1 strengthens coherence with EU competitiveness and internal market objectives by improving framework conditions through faster permitting, regulatory clarity and skills measures. It aligns well with the Digital Decade Policy Programme, industrial policy and climate objectives, as it does not mandate new capacity or alter environmental standards and raises no new State aid or competition concerns.

Policy Option 2 shows the strongest alignment with the EU's evolving strategic agenda, including the European Economic Security Strategy, STEP and the Competitiveness Compass. By combining framework measures with Strategic Projects and demand-side instruments, it enhances coherence with EU funding programmes and investment priorities. Targeted support creates potential trade-offs with competition and State aid principles, but these are mitigated through EU-level coordination and compliance with existing State aid rules. Increased manufacturing activity may raise energy demand, requiring consistency with climate and energy policies.

Coherence with international commitments. All options are consistent with the EU's international commitments, including WTO rules. The baseline and Policy Option 1 rely on non-discriminatory framework measures. Policy Option 2, while more interventionist, remains compatible with trade rules by focusing on resilience, innovation and security of supply without introducing discriminatory or trade-restrictive measures.

	Effectiveness in meeting objectives			**Efficiency**	**Coherence**
	SO1: Enhance the EU's capacity and security in mainstream and advanced chips, including AI chips	**SO2**: Develop a strong user market across key industry sectors	**SO3**: Increase intelligence capabilities for crisis preparedness and response		
PO0 (BAU):	0	0	0	0	0
PO1	+	+	++	++	++
PO 2	+++	++	++	+++	++ +

Legend: 0 no / neutral impact; + minor positive impact; ++ positive impact; +++ significant positive impact; - minor negative impact; -- negative impact; --- significant negative impact

8 PREFERRED OPTION

8.1 Reasons for the preferred option

The revision of the Chips Act takes place in a context of geopolitical challenges for the EU, persistent supply chain vulnerabilities and rapid technological developments, particularly in AI. As set out in Chapter 2, the Union continues to rely heavily on a small number of non-EU actors for semiconductor design and manufacturing capabilities. These overdependencies have already resulted in disruptions with significant economic and societal impacts. At the same time, the EU lacks sufficient tools to anticipate and manage semiconductor supply shocks**.** As Call for Evidence respondents consistently emphasised that there is need for

sustained, long-term strategic commitment at Union level to achieve the EU's ambitions in this sector - reinforcing the assessment that incremental or short-term measures are insufficient to address structural vulnerabilities in the value chain.([208]) **Policy Option 2 is the preferred option because it provides a coherent and ambitious albeit proportionate response to these structural challenges.**

Policy Option 2 strengthens and extends the current Chips Act through three mutually reinforcing components: **EU-co-funded Strategic Projects, targeted demand-side measures and a more robust monitoring and crisis-preparedness framework**. These measures address the core problems identified, namely the EU's overdependence on third-country suppliers and its insufficient supply chain intelligence capabilities, and they help establish the conditions for a more competitive, resilient and sovereign semiconductor ecosystem.

Strategic Projects would help to bolster the Union's capacities in critical segments of the value chain. While the initial Chips Act has triggered multiple investments the Union maintains precarious technological dependencies. **Strategic Projects provide a coordinated Union framework** to mobilise and pool resources for facilities of strategic European relevance, including leading-edge manufacturing, advanced packaging, specialised foundries, design capacity and key upstream supply chain segments. By reducing financing risks an ensuring cross-border spillovers and coherence, these projects respond directly to the structural gaps identified in the problem analysis and are central to increasing capacity, competitiveness and technological sovereignty.

Secondly, there are demand-side instruments, **notably innovative procurement and procurement of chips**. These measures respond to a structural weakness of the EU economy, whereby its main industries consume significant volumes of semiconductors - predominantly of mature technologies - while generating only limited direct demand for the advanced chips that drive global investment decisions. Much of the Union's consumption of leading-edge chips is embedded in imported systems, limiting the business case for locating advanced manufacturing and design activities in Europe. AI is expected to change this with demand for AI chips for AI Factories, Gigafactories and datacentres rising at a steep rate. By providing predictable early offtake for strategically important chips, demand-side measures reduce utilisation risks in the ramp-up of new facilities and accelerate technological uptake in key user industries such as automotive, industrial automation, robotics, telecoms and defence. This supports the emergence of a stronger internal market for advanced semiconductors and reinforces Europe's broader industrial competitiveness as set out in Annex 5.

The third component concerns **monitoring and crisis preparedness**, an area where the evaluation identified clear shortcomings. Despite progress under Pillar III of the current Chips Act, voluntary and ad-hoc information collection has not provided the effectiveness required to anticipate risks or coordinate timely responses. The preferred option therefore establishes a **Business-to-Business Semiconductor Supply Chain Platform**, supported by the possibility for the Commission to **use requests for information**. This framework enables continuous access to risk-relevant data, including information on dependencies and single points of

([208]) Annex 2 Stakeholder Consultation (Synopsis Report).

failure, **under strict confidentiality safeguards and EU antitrust compliance**. It strengthens the Union's capacity to detect, assess and mitigate disruptions and to coordinate measures across Member States. This enhanced intelligence function is essential to ensuring the Union's economic security in an increasingly complex and contested global environment. Overall, Policy Option 2 provides the most coherent and effective pathway to achieving the general objectives of the Chips Act 2.0: strengthening Europe's semiconductor competitiveness[209] and resilience and reinforcing the Union's capacity to anticipate and manage supply chain crises. It does so by addressing the root causes identified in the problem analysis and by providing targeted solutions for each of the four specific objectives. *Strategic Projects* directly address the EU's missing or insufficient capacities in key segments of the value chain (SO1). By reducing investment risks and aligning national and Union-level initiatives, they also improve the European investment environment (SO3), enabling projects that would otherwise not materialise under current legislation. Demand-side measures complement this by stimulating early and predictable uptake of advanced semiconductor technologies in Europe's major user industries (SO2). Here, reaching the set target of EUR 5 billion in innovation procurement would enable the validation of European technologies which are currently unavailable on the market and thus giving user industries the possibility to procure indigenous solutions. These instruments help overcome the EU's weak market pull for leading-edge chips, shorten time-to-market for innovative products and strengthen the interdependence between EU-based manufacturing and downstream user industries.

The enhanced monitoring and crisis-preparedness framework addresses the Union's gap in granular and timely information that limits its ability to detect vulnerabilities and coordinate responses (SO4). The **Business-to-Business Semiconductor Supply Chain Platform** provides the intelligence required for effective early-warning, preparedness and mitigation strategies.

The preferred option is consistent with Articles 173(3) and 114 TFEU, as its core measures address challenges that Member States cannot resolve alone without fragmenting the internal market. Strategic Projects require EU-level coordination and pooled funding to ensure that new manufacturing, design and packaging capacities strengthen the Union's strategic position in a coherent and complementary manner, avoiding duplication of efforts. Likewise, demand-side instruments function effectively only at Union scale; without common frameworks, divergent national incentives would risk distorting competition and weakening the internal market for advanced technologies.

The enhanced monitoring and crisis-preparedness framework reflects the need for Union action: semiconductor supply chains are cross-border, and only an EU-level Platform can provide the integrated visibility necessary for timely and proportionate responses. These measures are proportionate, as they introduce obligations only where voluntary cooperation has proven insufficient, target well-defined market failures and apply strict safeguards to information requirements. The Call for Evidence respondents called for strengthened industry–government dialogue and a more prominent role for the ESB to improve strategic coordination. This feedback supports the governance enhancements envisaged under the

[209] For further information, see Annex 5.

preferred option, including improved coordination, transparency and preparedness, without fundamentally altering the institutional architecture.

The expected impacts of the preferred option reflect its targeted and strategic nature. Economically, it supports the **deployment of critical manufacturing and design capabilities**, enhances ecosystem depth and reduces disruption-related losses through strengthened intelligence. Socially, it contributes to the creation of **highly skilled employment with high wages** and creates **improved conditions for innovation**, including for SMEs and start-ups. Environmentally, while expanded capacity increases absolute resource use, new facilities are expected to operate with higher efficiency.

8.2 Implementation

8.2.1 Strategy for implementation

For the Union to address its dependencies it must take a two-fold approach:

- **Strengthen our strengths** – delivered by the first Chips Act, which mobilised EUR 80 billion in manufacturing investments aligned with the needs of European user industries, and reinforced Europe's world-class Research and Technology Organisations through an unprecedented EUR 2.5 billion investment in pilot lines. This shall continue through the implementation of initiatives similar to the ones undertaken under the first Chips Act.
- **Venture into new markets** – by fostering a new generation of European semiconductor companies and helping them scale. This is increasingly important as AI and robotics diffuse across society and industry. Meeting the resulting demand for compute, both in centralised data centres and at the edge, will create new markets and application areas. Capturing these opportunities will depend on disruptive innovation, which is typically difficult for incumbents to deliver at speed. By venturing into new markets across the semiconductor value chain, particularly for more leading-edge technologies, the Union will then create the conditions for manufacturing capacity to increase which in turn would strengthen security-of-supply and resilience.

When operating in tandem, the tools set out in PO2, notably increased RDI investment (PM1), Strategic Projects (PM9) and Innovation Procurement (PM10) complemented by the existing measures under the Chips Act such as the Design Platform and the Chips Fund, create new opportunities to deliver the second part of the approach.

8.2.1.1 Scaling-up a new generation of European semiconductor market actors

The new measures proposed in PO2 allow for the creation of new companies and the de-risking of development of new technologies across the value chain from specialised materials to design to the deployment of process technology in new foundry capacity. This is a vital pre-requisite to re-instil dynamism into the European semiconductor ecosystem.

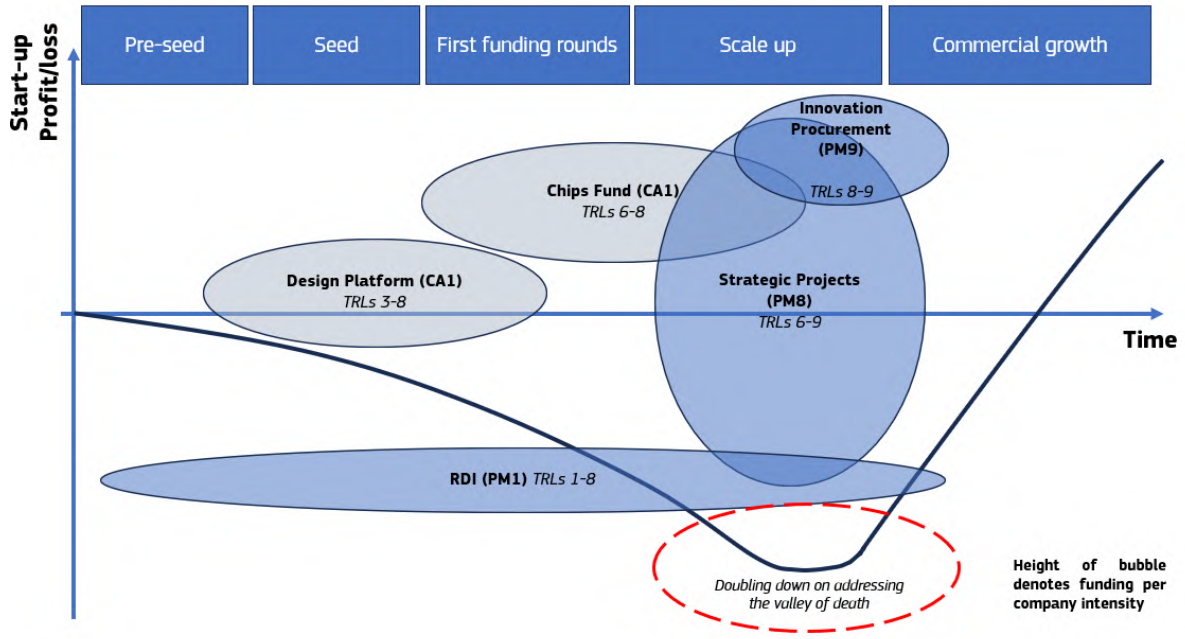

Figure 20 - Chips Act 2: A more comprehensive toolbox for scaling up semiconductor start-ups

The measures proposed in Chips Act 2 provide all the elements required for a concerted European effort to support a sovereign semiconductor industry - starting from research (**PM1**) to industrial deployment via Strategic Projects (**PM8**) and eventually also demand stimulation via innovation procurement (**PM9**).

These measures can be applied to a wide variety of contexts, but for the sake of example, they will be applied for the case of the development of a sovereign European AI Inference chip. A potential approach is foreseen as follows:

PM1 would support basic and applied research in the development of new breakthrough technologies, and foster innovation, addressing different computing paradigms and process technologies.

Once this technology is proven to a sufficient level, industrialisation could be potentially supported as a Strategic Project via **PM8**. Eventually support for innovation procurement via **PM9** would be granted, which creates predictable demand with anchor customers and enables reference deployment of EU chips in strategic segments, starting with AI Factories and Gigafactories driving internal demand for advanced AI chip design. At the same time, industrial accelerators will convert pilot-line outputs into user-ready solutions. The above can be applied to different sectors, such as automotive, defence, telecom and critical infrastructure.

Public authorities may also prioritise the procurement of this sovereign solution via non-market criteria in **PM10**, creating a structural premium for secure supply and protecting EU downstream sectors from future dependency risks.

With sufficient private co-investment and buy-in (which would always be the vast majority of investment), such a combination of measures would represent a complete system of intervention that could lead to the nurturing of commercially viable European solutions.

With sustained investment, a critical mass of emerging semiconductor companies could be built. These firms would be positioned to seize the opportunities set out in Section 1.1 and to capture demand from an era of expanding AI data-centre capacity and the mass adoption of robotics.

As seen in **Figure 21,** data centre demand is expected to increase at a rate of 12% per year – reaching 62GW in 2036. Taking a general assumption that one GPU consumes approximately 1kW of energy ([210]) – this would imply around 62,000,000 chips which represents a significant demand that could potentially be tapped into by European actors.

Furthermore, the ongoing deployment of AI Factories and the planned investment in AI Gigafactories, backed by the EUR 20 billion in the InvestAI facility and envisaged to support up to five facilities, are another example of upcoming deployment of AI compute infrastructure. Under this initiative, the ambition is to deploy 5 datacentres with 100MW of compute capacity each.

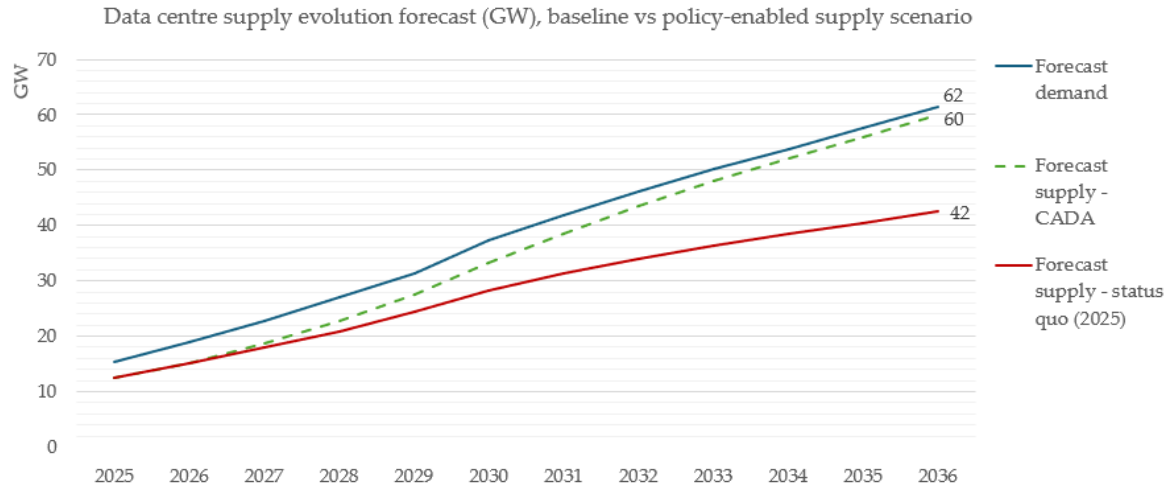

Figure 21 - Evolution of the gap between data centre demand and supply (figures in GW) Source: Technopolis

The AI Gigafactories as a publicly steered initiative can serve as an important vehicle for the validation of European technologies. Here, **PM9** may be deployed for the procurement of experimental European technology for validation purposes through pre-commercial procurement and public procurement of innovation. Should 5% of the capacity of the AI Gigafactories be dedicated to the validation of European solutions, this would serve as an opportunity to deploy 25 MW of compute capacity that is European sourced.

[210] Nvidia turns up the AI heat with 1,200W Blackwell GPUs | The Register

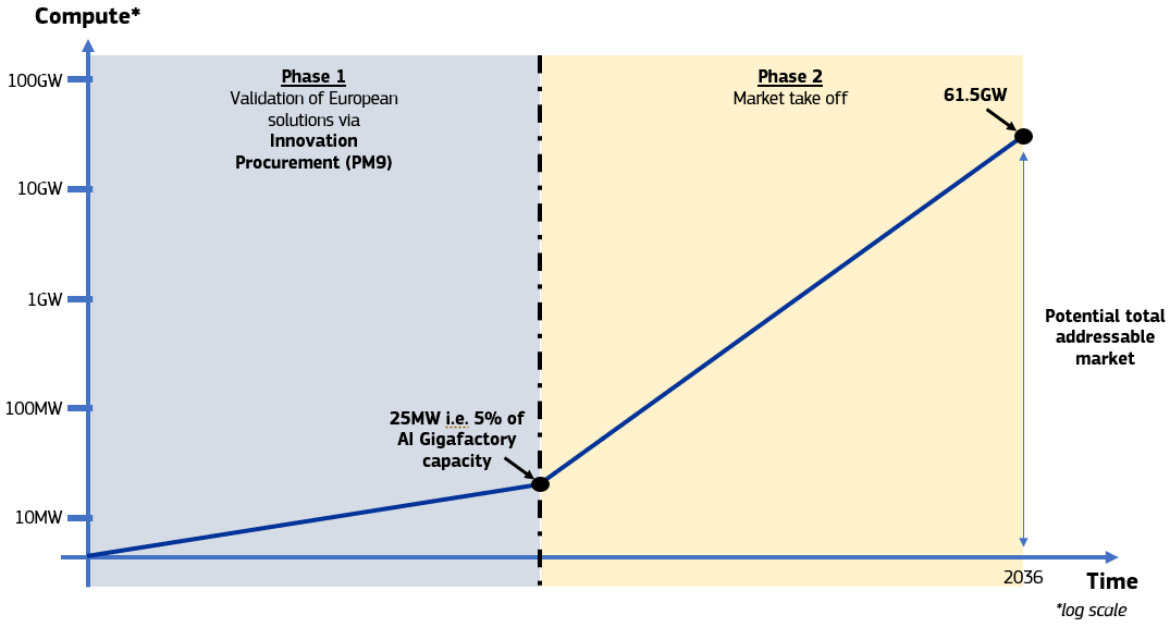

Figure 22 - Uptake of sovereign EU AI compute

This validation would then in turn give these market actors credibility on the market which can be used to pursue the larger EU data centre market and also compete globally.

8.2.1.2 Embedding resilience – selective investments on crucial components of the value chain

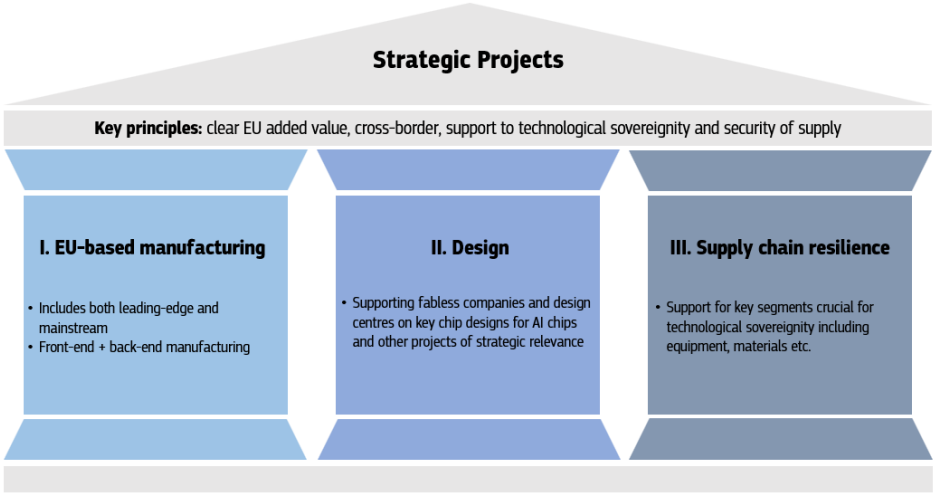

Figure 23 - Architecture of Strategic Projects (PM9)

As set out above, the EU, despite some strengths, has significant dependencies across all the semiconductor value chain. Re-shoring the entire value chain, is neither realistic nor desirable and therefore this necessitates that choices are made.

Crucial amongst these is the lack of leading-edge front-end manufacturing capacity and an advanced packaging facility together with some meaningful manufacturing capacity in memory technologies in Europe which are core-components of an AI value chain. Addressing

such vulnerabilities shall be a principal pursuit when implementing the revised Chips Act for two reasons:

8.2.1.2.1 Crucial strategic importance

Firstly, supply disruption of these semiconductors would deny Europe the possibility to deploy crucial AI infrastructure, both at the edge and in the data centre, which in the medium term will be of vital importance for the maintenance of economic growth and the functioning of essential societal services and industry.

Furthermore, the increasingly differentiating factor that this technology could have when it comes to security and defence, including cybersecurity, means that lack of sovereign access may render Europe vulnerable to violations of public order and security.

8.2.1.2.2 Market opportunity

Secondly, this segment of leading-edge technologies is the fastest growing segment in the semiconductor market. It is the driver of unprecedented growth in the industry that is expected to reach USD 1 trillion in revenues by 2026, an acceleration of 4 years from the consensus of market analysts. **Europe's lack of participation in this segment is resulting in a rapid loss of market share and risks rendering the EU irrelevant in the global semiconductor market**.

Recent evidence indicates that leading-edge AI chip markets are characterised by short-run capacity constraints and limited price responsiveness. For example, advanced 2.5D packaging capacity, particularly TSMC's Chip-on-Wafer-on-Substrate (CoWoS) platform used for frontier AI chips, has been reported as sold out through 2025 and into 2026, with oversubscription at least until mid-2026.([211])When it comes to front-end manufacturing, it is expected that foundry capacity will be scarce until at least end of 2027 and will probably persist as data-centre and AI compute demand increases exponentially, with foundries not being able to keep abreast.

Category	Logic node	Product	2026 Q1	2026 Q2	2026 Q3	2026 Q4	2027 Q1	2027 Q2
Logic	≤2nm	Accelerator	90	80	72	76	80	84
Logic		CPU	77	75	73	77	81	87
Logic	5/4/3nm	Accelerator	74	76	80	85	89	93
Logic		CPU	76	80	87	90	92	94
Logic	7nm	Miscellaneous products	82	81	79	81	84	86

Figure 24 - Percent of supply versus demand for semiconductors (Source: IBS)[212]

([211]) Fusion Worldwide. (2025). *Inside the AI bottleneck: CoWoS, HBM, and 2/3nm capacity constraints through 2027*. https://info.fusionww.com/blog/inside-the-ai-bottleneck-cowos-hbm-and-2-3nm-capacity-constraints-through-2027

([212]) IBS, Global Semiconductor Industry Service February 2026 - Analysis of Semiconductor Shortages.

Therefore, given multi-year expansion lead times, short-term output is effectively capacity-bound. In such conditions, price increases do not rapidly translate into higher quantities, implying a steep short-run supply curve. Demand has also proven resilient: despite elevated prices during the constraint phase, deployment of frontier AI hardware did not materially contract, suggesting limited short-run substitutability and strong willingness to pay among cloud vendors and AI companies.

Furthermore, investment in manufacturing capacity via Strategic Projects for more mature technologies that are of critical importance for certain user industries such as automotive and security and defence will be pursued to continue building resilience for European user industries.

8.2.2 Budget

All funding assumptions are without prejudice to ongoing negotiations related to the next Multiannual Financial Framework (MFF) for 2028-2035. The considerations made in the Impact Assessment are in line with the Commission proposal for the next MFF.

It is assumed that Member States are willing to co-fund. This is a reasonable assumption given the level of attention the topic has received, including the adoption of national strategies in over 10 Member States. ([213]) This assumption is also based on previous budget allocations by Member States over the course of the current MFF (2021-2027).

Considering the nature of the initiative, effectiveness is tied to the capacity of public authorities, including the Commission, to invest. The funding from the Union is also subject to the specificities of the upcoming Council regulation establishing the Joint Undertakings. The preferred option (PO2) is based on the assumption that the Union will be able to mobilise sufficient funding for an impactful application of the new policy measures foreseen under the proposed Chips Act. Of course, an important change in this revision will be the role of the Union in supporting strategically important manufacturing facilities. This would require at least an order of magnitude larger EU budget for semiconductors in the next MFF. Should these budgets not be realisable, then the impacts described in Section 6.2 will be more subdued.

8.2.3 Total cost benefit overview

The preferred option is expected to generate substantial economic returns across the semiconductor value chain, with EU manufacturers projected to achieve **EUR 6.6–11.5 billion (for total of EUR 40 billion public private funding)**([214]) in additional annual manufacturing revenue from Strategic Projects, while demand-side measures stimulate further design-related activity and crowd in private investment (see Annex 4). Public authorities stand to benefit from a significantly strengthened governance architecture, including, for the first time, direct EU co-financing of industrial deployment via the ECF, alongside new

([213]) Austria, Czech Republic, Finland, France, Germany, Ireland, Italy, Netherlands, Poland, Portugal, Spain.
([214]) The EUR 40 billion figure is provided for illustrative purposes only.

resilience capabilities that would allow the industry to identify supply chain bottlenecks before the crisis thresholds set out in the Chips Act are reached.

The total costs associated with the preferred option are proportionate and are substantially outweighed by the projected economic benefits, improved supply chain resilience, with SMEs fully exempt from reporting obligations.

Society at large would stand to benefit from improved continuity of essential services during supply disruptions, reduced exposure to geopolitical coercion, the creation of at least **7,300 direct and 36,500 indirect jobs,** and, over time, greater product choice and more competitive pricing for all downstream users of semiconductors. Further information can be found in Annex 3.

8.3 REFIT (simplification and improved efficiency)

The preferred option introduces targeted new obligations but also delivers notable simplification and efficiency gains for businesses and public administrations.

8.3.1 Simplification benefits

The preferred policy option (PO2) delivers simplification by introducing a coordinated EU-level framework in the case of Strategic Projects. With a single project pipeline for large-scale semiconductor investments, duplication of administrative steps and repetitive documentation are prevented. The clarification of the First-of-a-Kind label further simplifies State aid procedures for both Member States and companies. Additionally, the revised Chips Act will delete the concept of a European Chips Infrastructure Consortium (ECIC) for streamlining purposes as it was never used during the implementation of the Chips Act.

Another efficiency gain stems from faster and more predictable permitting procedures. Permitting and design phases for advanced semiconductor facilities in the EU are on average 7.5 months longer than in key competing jurisdictions. Assuming that each year of delay adds around 5% to the total project value, this implies an additional cost of approximately 3.125% of overall investment, corresponding to around EUR 625 million for a representative EUR 20 billion advanced fabrication plant. ([215]) By reducing iterative exchanges with authorities and clarifying permitting pathways, PO2 generates substantial implicit cost savings that outweigh compliance-related costs. Another simplification benefit arises from replacing ad hoc crisis-driven information requests with a structured **Business-to-Business Semiconductor Supply Chain Platform** reducing duplication and improving coordination across Member States. ([216])

8.3.2 Administrative impacts (OIOO perspective)

From a One-In-One-Out perspective, PO2 introduces limited new administrative burdens, largely offset by structural simplification. New "INs" for businesses consist primarily of disclosures of supply chain vulnerabilities, estimated at up to 10 person-days per request,

([215]) Annex 3, Table III (Application of the 'one in, one out' approach).
([216]) Annex 3, Table I – Improved visibility of supply chain vulnerabilities.

corresponding to approximately EUR 2,783 per large firm, with total costs of up to EUR 1.34 million per request in a full-coverage scenario. ([217]) These burdens are counterbalanced by "OUTs" in the form of fewer urgent and duplicative crisis-related data calls, streamlined information exchange and reduced internal monitoring effort through partial outsourcing of market-intelligence activities to the Platform. Businesses face a net administrative burden, consisting of onboarding the Platform and disclosures. However, these will be largely offset by the security of supply that this data sharing will enable. Additionally, assessments will only be made on a qualitative basis outside of a formal crisis in the first stage. Overall, PO2 results in a small net administrative burden, which is proportionate, REFIT-compliant and clearly outweighed by the simplification and efficiency gains delivered.

Better alignment of IPF/OEF procedures for projects that receive public funding and meet the requirements reduces administrative burden, shortens timelines, and enables Member States and the Commission to allocate resources more efficiently.

9 HOW WILL ACTUAL IMPACTS BE MONITORED AND EVALUATED?

The Commission will be responsible for monitoring the implementation of the intervention on a regular basis, possibly with the support of external studies, Member States and market data. Furthermore, the Commission will carry out a comprehensive evaluation of the effectiveness, efficiency, coherence, proportionality, and subsidiarity of Chips Act 2. **An evaluation report** presenting the main findings will be submitted to the European Parliament, the Council, the European Economic and Social Committee, and the Committee of the Regions within **four to five years** of the act entering into force. Where appropriate, the Commission may accompany this report with proposals for improving or adapting the Chips Act 2.0.

This review mechanism follows the approach established under the first Chips Act, ensuring continuity, comparability of results, and a long-term perspective on policy results. The Commission, in close cooperation with the Member States, will regularly monitor the implementation and application of the legal provisions, with particular attention to the effectiveness of the adopted measures. Monitoring activities will rely on quantitative and qualitative indicators, drawing from data provided by stakeholders across the semiconductor value chain, Member States, and relevant EU bodies. The overall success of the initiative will be assessed through evidence of strengthened **security of supply**, including progress in relevant measurable aspects such as the EU's share of global semiconductor production and changes in market concentration. The implementation of Chips Act 2.0 itself and its accompanying measures will also allow for systematic tracking of specific objectives, expected benefits, and related impacts.

9.1 Measurable indicators to monitor the implementation and to report on the progress of the initiative towards the achievement of its objectives

The proposed indicators build on the two new general and specific objectives of the Chips Act 2.0.

([217]) Annex 3, Section II and Table III.

Monitoring indicator for general objectives:

- Total semiconductor related FDI inflows into the EU;
- Skilled workforce in semiconductor and photonics, including workforce trained or reskilled through the competence centres under Pillar I;
- Public support for start-ups and scale ups;
- Scale-up funding via private equity and venture capital.

Monitoring indicators for specific objectives

SO1: Enhance the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips

The first specific objective seeks to enhance the EU's capacities and security of supply for semiconductors in sectors relevant for the Union's economic security and competitiveness by steering larger and more targeted public and private investments.

Monitoring indicator for SO1:

- EU share of global semiconductor revenues (in EUR) in different segments of the value chain including:
  - Design, IP, EDA
  - Manufacturing
  - Equipment manufacturing
  - OSAT (packaging)
  - Materials / gases
- Top European firms in any value chain segment.
- Operational wafer fabrication capacity in the EU (wspm).

SO2: Develop a strong user market across key industry sectors

The second specific objective is designed to ensure the emergence of a robust and innovative end users' market in the Union ready to adopt new advanced semiconductor technologies, notably for AI chips.

Monitoring indicator for SO2:

- Consumption of chips by key sectors (automotive, energy, health, defence, telecom, AI/data centres/cloud) in value (EUR).

SO3: Increase intelligence capabilities for crisis preparedness and response

Finally, increasing monitoring capabilities should ensure EU's agile, effective, and proactive response prior to a semiconductor crisis. When the EU's economic security is at risk, real-time information and data from companies across the semiconductor supply chain and end-user markets can provide critical insights and enable mitigation or emergency measures at Union or national level.

Monitoring indicator for SO3:

- Coverage by the Business-to-Business Semiconductor Supply Chain Platform (in %) of the Union semiconductor value chain.