

Council of the European Union

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COVER NOTE

From:	Secretary-General of the European Commission, signed by Mr Jordi AYET PUIGARNAU, Director	
date of receipt:	19 November 2018	
То:	Mr Jeppe TRANHOLM-MIKKELSEN, Secretary-General of the Council of the European Union	
No. Cion doc.:	C(2018) 7499 final - Annex	
Subject:	ANNEX to the Commission Delegated Directive amending, for the purposes of adapting to technical progress, Annex III to Directive 2011/65/EU of the European Parliament and of the Council as regards an exemption for lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages	

Delegations will find attached document C(2018) 7499 final - Annex.

Encl.: C(2018) 7499 final - Annex



EUROPEAN COMMISSION

> Brussels, 16.11.2018 C(2018) 7499 final

ANNEX

ANNEX

to

Commission Delegated Directive

amending, for the purposes of adapting to technical progress, Annex III to Directive 2011/65/EU of the European Parliament and of the Council as regards an exemption for lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

<u>ANNEX</u>

"15	Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages	 Applies to categories 8, 9 and 11 and expires on: 21 July 2021 for categories 8 and 9 other than in vitro diagnostic medical devices and industrial monitoring and control instruments; 21 July 2023 for category 8 in vitro diagnostic medical devices; 21 July 2024 for category 9 industrial monitoring and control instruments, and for category 11.
15(a)	Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies:	Applies to categories 1 to 7 and 10 and expires on 21 July 2021."
	 a semiconductor technology node of 90 nm or larger; 	
	 a single die of 300 mm² or larger in any semiconductor technology node; 	
	 stacked die packages with die of 300 mm² or larger, or silicon interposers of 300 mm² or larger. 	

In Annex III, entry 15 is replaced by the following: